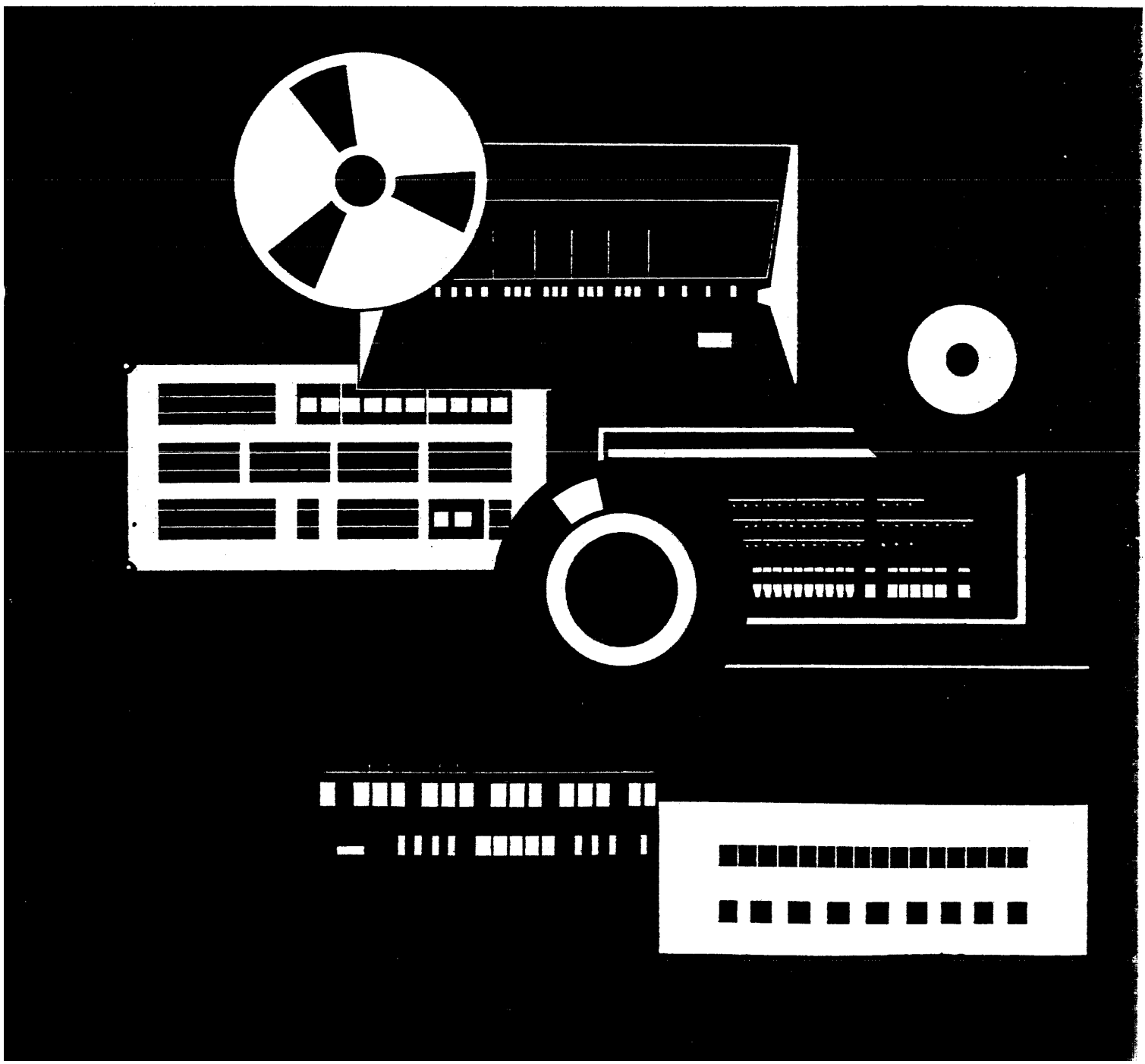
DATUM PERIPHERAL EQUIPMENT DIVISION

SERIES 5091 MAGNETIC TAPE FORMATTER SYSTEMS



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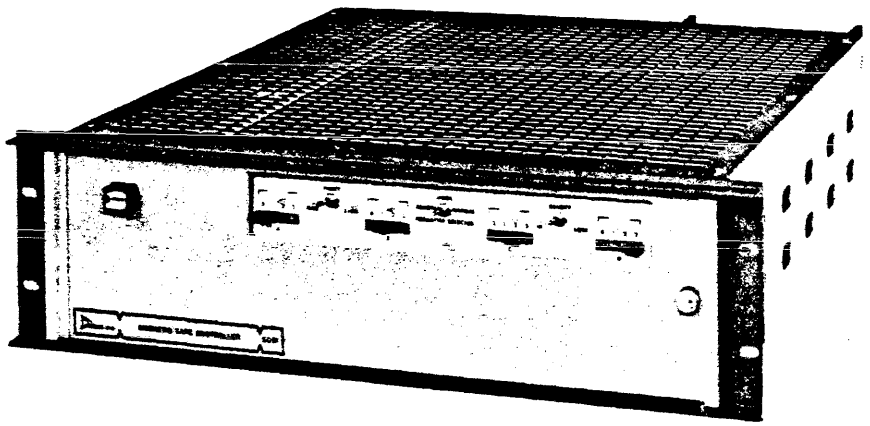


- **Selection of NRZ or phase-encoded formats with or without computer adapter interfaces and software**
- **Availability of adapters for a wide range of mini-computers**
- **Control of as many as eight 7- and/or 9-track tape units (four per formatter)**
- **Compatibility with computer software while handling seven- or nine-track, multiple-speed, multiple-density tapes**
- **Expandability in the field simply by adding logic cards**
- **Front-panel controls and indicators**
- **Internal power supply adequate for any desired configuration**
- **DTL/TTL IC formatter logic to assure maximum compatibility**
- **Availability of blank circuit cards for "design your own" adapter**
- **Etched circuitry for highest reliability**

The DATUM Series 5091 Magnetic Tape Formatters satisfy all requirements for tape-control in mini-computer installations. The result of years of mini-computer interface experience, the 5091 Series consists of controls, cabinet, chassis and power supply and the formatters and computer adapters for which they provide slide-in accommodation. Whether the need be for a Formatter, for a Formatter with provision for a user-designed Computer Adapter or for a complete Tape Controller, the DATUM Series 5091 will provide the ideal instrumentation.

This modularly designed series generates and reads IBM-compatible NRZ and phase-encoded formats and, with the addition of a Computer Adapter, will control as many as eight magnetic tape units. If desired, off-the-shelf Computer Adapters and software are available that will accommodate 90% of the commercially-available mini-computers.

The Series 5091 design concept, a product of DATUM's wide experience in interfacing with different mini-computers, permits a high degree of compatibility with the hardware/software designs of the various computer manufacturers and with existing user-developed software. When ordered with a Computer Adapter installed, the 5091 instrument thus becomes a Tape Controller system custom-designed, both in hardware and software, to the mini-computer with which it is to function.

FRONT-PANEL CONTROLS AND INDICATORS

TAPE UNIT SELECT switches allow any unit number (0, 1, 2, 3) to be assigned to any tape unit (A, B, C or D). **MODE** switch allows manual override control over parity and density selection for seven-track tape units in addition to standard program control. **PARITY** switch allows selection of ODD or EVEN parity. **DENSITY** switch allows selection of HIGH or LOW density. **VISUAL INDICATORS** display the tape unit, formatter, parity and density selected.

EQUIPMENT CONFIGURATIONS

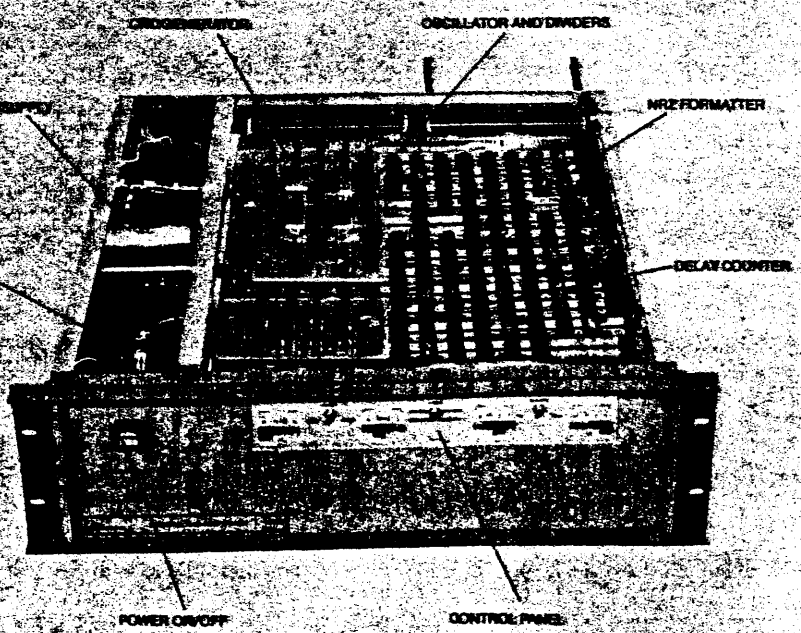
The basic Series 5091 Controller/Formatter will house and power three large circuit-cards. One card slot is required for NRZ formatting, two card slots are required by the Phase-Encoding Formatter, and one card slot is necessary for the Computer Adapter. Therefore, two enclosures are necessary for some configurations.

SYSTEM CONFIGURATION	FORMATTERS REQUIRED: NRZ	FORMATTERS REQUIRED: PHASE ENCODED*	COMPUTER ADAPTER	ORDER DATUM NUMBER
One to four 7- and/or 9-track NRZ tape units	One		Customer-Supplied	5091-1
One to four 9-track 1600 PE tape units		One*	Customer-Supplied	5091-2
One to eight 7- and/or 9-track NRZ tape units	Two**		Customer-Supplied	5091-3
One to eight 9-track 1600 PE tape units		Two**	Customer-Supplied	5091-4***
One to four 7- and/or 9-track NRZ and One to four 1600 PE tape units	One**	One*	Customer-Supplied	5091-5
One to four 7- and/or 9-track NRZ tape units	One		One	5091-6
One to four 9-track 1600 PE tape units		One*	One	5091-10
One to eight 7- and/or 9-track NRZ tape units	Two**		One	5091-7
One to eight 9-track 1600 PE tape units		Two**	One	5091-8***
One to four 7- and/or 9-track NRZ tape units; one to four 1600 PE tape units	One**	One*	One	5091-9***

*Uses two card slots. **Two Formatters daisy-chained to a single Computer Adapter.
***Requires two enclosures.

SPECIFICATIONS

SIZE: 5-1/4" high, 19" (RETMA rack) wide, 24" deep.
WEIGHT: 25 lbs.
POWER SOURCE: 117 volts ± 10%, 60 Hz.
TEMPERATURE RANGE: 0° – 50°C.
HUMIDITY RANGE: 0% to 95%, non-condensing.



5091 MAGNETIC TAPE FORMATTER

SPECIAL "DESIGNED-BY-DATUM" FEATURES

1. **PROVEN HARDWARE AND SOFTWARE.** DATUM has delivered more than 150 complete computer-interfaced systems that included computer adapters and software. Typical computers interfaced are:

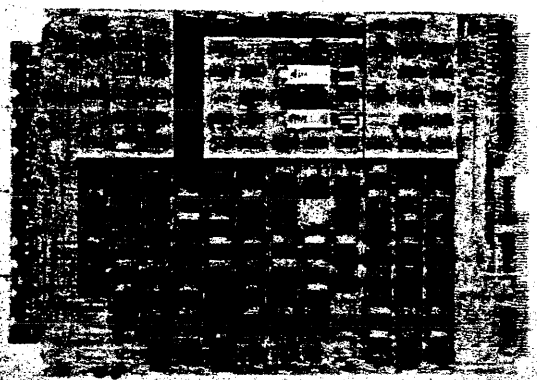
   Computer Automation 816; **Data General** Nova; **Digital Equipment Corp.** PDP-8, 8/e, 8/i, 8/L, 9, 9/L, 11, 12, 15; **Hewlett-Packard** 2114, 2115, 2116; **Honeywell** H316, H416, H516, H124A; **IBM** 1130; **Microsystems** 810; **SDS/XDS** CE16, CF16; **Varian** 620/i.

2. **DESIGNED-IN SOFTWARE COMPATIBILITY.** Multiple record spacing with one command; Single-command erase-then-write; Seven-track filemark in nine-track mode control, BCD 10-to-zero conversion control.

3. **PROFIT BY OUR EXPERIENCE.** If you will be designing your own Computer Adapter, you will find that the features already designed into the DATUM Formatter will save you as many as 25% of the chips you would normally require in your Computer Adapter.

4. **FRONT PANEL INDICATORS, UNIT-SELECT SWITCHES AND PARITY/DENSITY SWITCHES.**

5. **NO ADJUSTMENT POTENTIOMETERS. NO ONE-SHOTS.**



5091

NRZ FORMATTER

CIRCUIT BOARD.

OTHER ESSENTIAL OPERATING AND DESIGN FEATURES

SPECIAL BUFFER REGISTERS in the Formatter for Read and Write make data available for the entire period between Read strobes. They will also accept Write data at any time the computer outputs the character. No external storage registers are required in the user's computer adapter.

A MIX OF ANY TWO TAPE SPEEDS can be accommodated by one Formatter — within a range of 6.25 to 112.5 inches per second. Compatible with entire PEC or Wang tape-unit lines. Special speeds easily handled.

A MIX OF DIFFERENT HIGH/LOW DENSITY PAIRS of 7-track units on one NRZ formatter. For example, one transport could be 800/556 bpi, a second transport could be 556/200 bpi.

"DATA TRANSFER TIMING ERROR" status bit presented to the interface if a Read or Write data transfer is not accomplished before the next "Read" or "Write" strobe occurs.

FORWARD OR REVERSE READING with complete error-checking in either direction.

FORMATTER DIRECTLY COMPATIBLE with all general-purpose-computer timing requirements. Interface control pulses can be a minimum of 100 nanoseconds wide. The Formatter internally interlocks control signals to the tape units.

CONTINUOUS READ OR WRITE CAPABILITY (gapping "on-the-fly") provided by the Formatter to optimize data transfer rates.

NO FREQUENCY ADJUSTMENTS ARE NECESSARY. Timing is referenced to a crystal-controlled oscillator followed by a divider chain that selects the desired frequencies. Any mixture of any two frequencies may be selected at the time of purchase. Since all delays are taken from this timing chain, no one-shots are used. **No adjust-pots are used.**

READ, WRITE AND MOTION CONTROL LOGIC included in the Formatter. **VRC, LRCC, CRCC** generated by the NRZ Formatter. VRC and LRCC checked. **FILE MARKS** written and recognized by Formatter.

SIMPLE TAPE UNIT EXPANSION in the field by adding additional tape units as they are needed.

TIMING FOR IBM-COMPATIBLE INTER-BLOCK GAPS and correct head positioning between records.

SINGLE GAP (write/read) **AND DUAL GAP** (read after write) transports can be "mixed."

FIXED-LENGTH ERASE COMMANDS and combination "erase then write" command provided by Formatter.

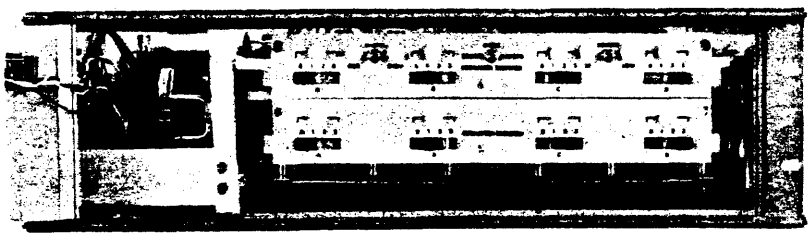
SOFTWARE COMPATIBILITY MAINTAINED with existing computer manufacturer's software, by providing ability to erase a three-inch gap and then, with one command, write a Record or File mark. Also with one command the user can space over any number of records, forward or backward.

NO LOCK-UP AT LOAD POINT when the Formatter is commanded to backspace or Read Reverse. Command rejected and Reject status returned to get attention of computer.

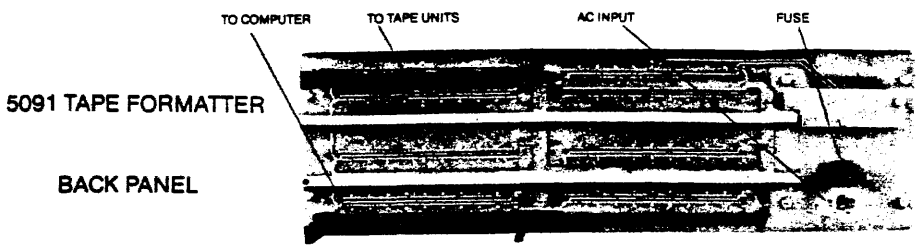
PHASE-ENCODED FORMATTER CONTAINS ALL LOGIC necessary to generate the pre-amble, post-amble, phase-encoded data and file mark patterns for recording. Read logic allows complete recovery of Read data, including data decoding, buffering, error and file mark detection and error correction.

IF YOU ARE TO DESIGN YOUR OWN ADAPTER...

TO ASSIST IN YOUR OWN COMPUTER ADAPTER DESIGN, blank printed-circuit boards are available with which to build your own Computer Adapter or logic card. These boards plug directly into the existing enclosure, which provides complete interconnection. The boards can be supplied with as many as 196 IC sockets already mounted. Further, to assist in the development of your Adapter logic and software, DATUM can provide logic diagrams and actual software.



5091 TAPE FORMATTER, PANEL OPEN, SHOWING NRZ FORMATTER BOARD (TOP) AND PHASE ENCODED FORMATTER BOARDS (BOTTOM) INSTALLED.



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SYSTEM CONFIGURATION	FORMATTERS REQUIRED		COMPUTER ADAPTER	ORDER DATUM NUMBER
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One to eight 7- and/or 9-track NRZ tape units	Two**		Customer-Supplied	5091-3
One to eight 9-track 1600 PE tape units		Two**	Customer-Supplied	5091-4***
One to four 7- and/or 9-track NRZ and One to four 1600 PE tape units	One**	One*	Customer-Supplied	5091-5
One to four 7- and/or 9-track NRZ tape units	One		One	5091-6
One to four 9-track 1600 PE tape units		One*	One	5091-10
One to eight 7- and/or 9-track NRZ tape units	Two**		One	5091-7
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*Uses two card slots. **Two Formatters daisy-chained to a single Computer Adapter.
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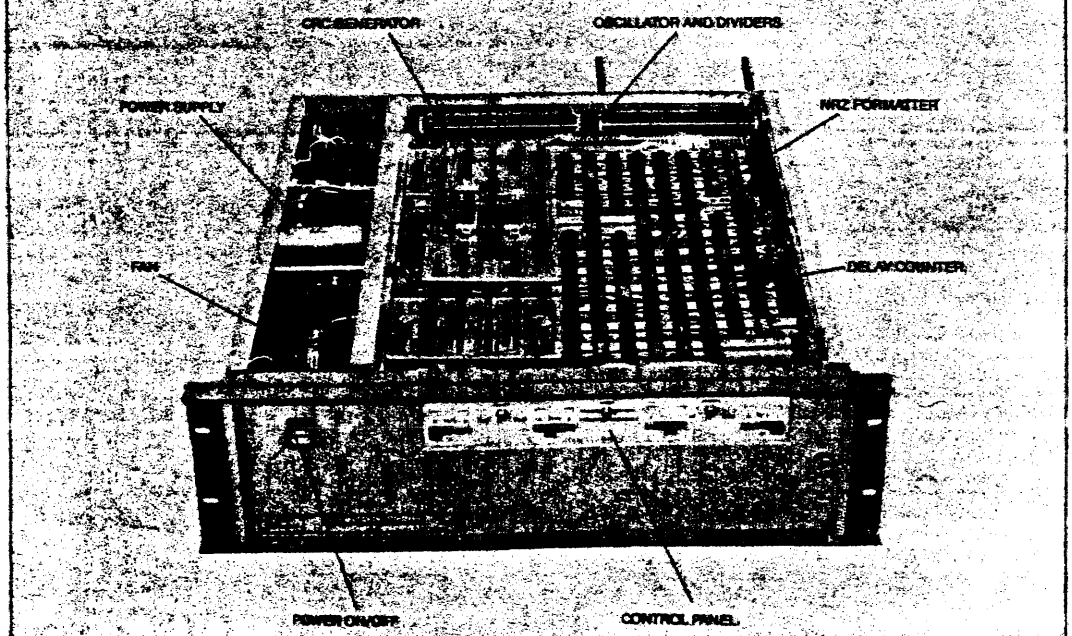
SPECIFICATIONS

SIZE: 5-1/4" high, 19" (RETMA rack) wide, 24" deep.
WEIGHT: 25 lbs.
POWER SOURCE: 117 volts ± 10%, 60 Hz.
TEMPERATURE RANGE: 0° – 50°C.
HUMIDITY RANGE: 0% to 95%, non-condensing.



5091 MAGNETIC TAPE FORMATTER

PERIPHERAL
EQUIPMENT DIVISION

MODEL 5091

1600PE FORMATTER

INSTRUCTION MANUAL

PUBLICATION NO. 1803.8

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INSTALLATION INSTRUCTIONS

MODEL 5091 FORMATTERS

1. UNPACKING AND INSPECTION OF FORMATTER

a. Visually inspect the Formatter to ascertain that there has been no physical damage. Should damage be observed, the carrier must be notified within ten days if an insurance claim is to be made.

b. Make certain that all boards are plugged firmly into the mother boards.

c. Make certain that the speed chip (Assembly 701587) is installed. On the NRZ units, the speed chip is located on the lower right-hand corner (F5) of the center board (Assembly 76134) of the three smaller boards mounted on the left side of the motherboard. On the Phase Encoded units, the speed chip is located on the lower right-hand corner (D28) of the left-most of the three smaller boards (Assembly 76191) mounted on the motherboard. Should the speed chip be removed and then replaced, be certain that pin 1 of the chip (the beveled corner) matches pin 1 etched on the circuit board.

d. Make certain that the main boards are seated firmly in the rear panel sockets.

2. MOUNTING THE FORMATTER

A small packet of mounting hardware containing 10-32 phillips-head screws, metal grommets and nylon chafing guards is included with each Formatter. The Formatter is mounted in the rack by lining its four mounting holes up with four threaded mounting holes in the rack and securing it with the grommet guards, grommets and 10-32 screws.

The Formatter requires 24" of rack space behind the mounting surface. This 23"-deep rack allows for cable bend at the rear of the Formatter.

3. MOUNTING THE TAPE UNITS

All tape units require rack mounting. Mounting of the tape units in a standard 19" RETMA rack is described in the tape unit manual. The 5091 Formatter and the tape units must be mounted such that five-foot tape-cable lengths will "daisy-chain" to all units. This requires that all units be mounted either directly above, below or beside the previous unit in the chain. (See sketch below.)

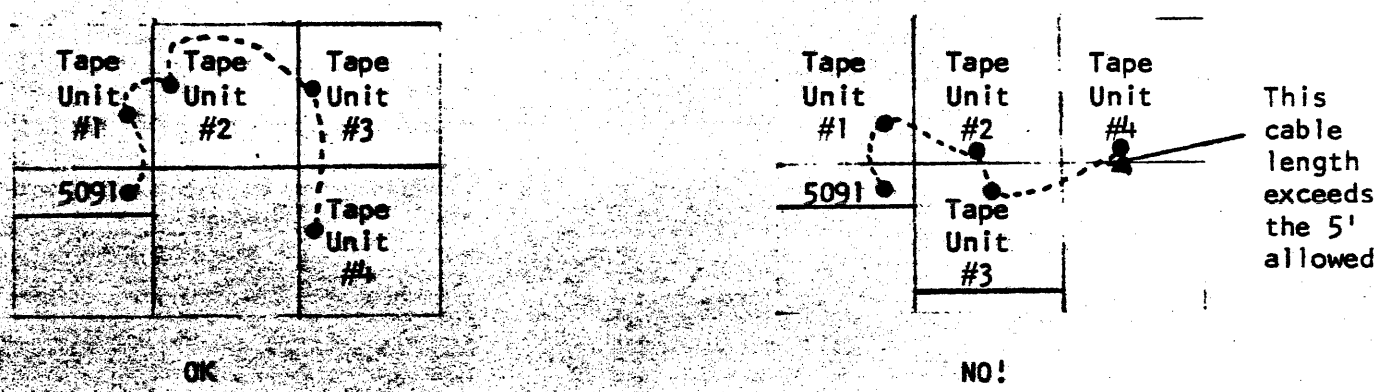


FIGURE 1

The standard multiple-tape-unit "daisy-chain" configuration requires termination resistors to be deleted from all but the last tape unit. Therefore, the power to the last tape unit must be switched to "ON" when any tape unit is in use. This supplies power to the terminator.

3.1 Tape Unit Termination Option

The Tape Unit Termination Option provides termination circuits on printed-circuit boards that plug onto the last tape unit. This Option enables power to be applied from any tape unit that has power "ON". Installation of this option allows termination resistors to be deleted from all tape units and allows operation to continue, even when the last tape unit becomes defective to the extent that its power cannot be turned on.

4. INSTALLATION, MODEL 5091 FORMATTER

The installation hardware consists of Cable 960076, the single-connector end of which attached, via P102, to J102, the upper-left-hand connector on the back panel of the Controller. Two 6/32 screws are supplied to secure this connection.

CAUTION: TO AVOID COSTLY DAMAGE TO EQUIPMENT, IT IS IMPERATIVE THAT THE CONNECTORS BE ATTACHED IN ACCORDANCE WITH THE FOLLOWING INSTRUCTIONS.

4.1 To WANG NRZ Tape Units (Figure 2)

1. Connector AP101 attaches to J16 on the Wang Tape Unit, which is the upper connector (marked "J16") on the second printed-circuit board from the left as you face the back of the Wang unit. As shown in Figure 1, make certain that the cable enters from the upper end of the connector and that the "A" stamped on the connector designates the end furthest into the tape unit.

2. Connector AP103 attaches to J6 on the Wang Tape Unit, which is the upper connector (marked "J6") on the right-hand board (as you face the back of the tape unit). Ascertain, as in Step 1, that the cable enters from the top end of the connector and that "A" is stamped on the connector-end furthest into the unit.

3. Connector AP102 attached to J1, which is the bottom connector on the board designated in Step 2. Ascertain that the cable enters the lower end of the connector and that "A" is atamped on the connector-end furthest into the unit.

4.2 To WANG PHASE ENCODED Units (Figure 3)

1. Connector P16 connects to jack J16 on the upper leading edge of the first printed circuit board from the left, as you face the back of the Wang unit. As shown in Figure 3, make certain that the cable enters from the upper end of the connector and that the "A" stamped on the connector designates the end furthest into the tape unit.

2. Connector P6 connects to jack J6 on the upper edge of the right-hand printed circuit board (as you face the back of the unit). See Figure 3. Ascertain that the connector-end stamped "A" is shown in the illustration.

3. Connector P1 connects to jack J1 on the lower edge of the right-hand circuit board. (See Figure 3.) Ascertain that the connector-end stamped "A" is shown in the illustration.

4.3 To PERTEC Units (Figure 4)

1. Connector AP102 attaches to J102, the top connector on the innermost (Read/Write) circuit board. Make certain that the end of the

connector stamped "A" is toward the top of the tape unit, which means that the cable enters the connector from below.

2. Connector AP103 attaches to J103, the bottom connector on the innermost (Read/Write) circuit board. Position the connector so that the end stamped "A" is closest to the bottom of the tape unit.

3. Connector AP101 attaches to J101, the bottom connector on the outermost (control) circuit board. Position the connector so that the end stamped "A" is closest to the bottom of the tape unit.

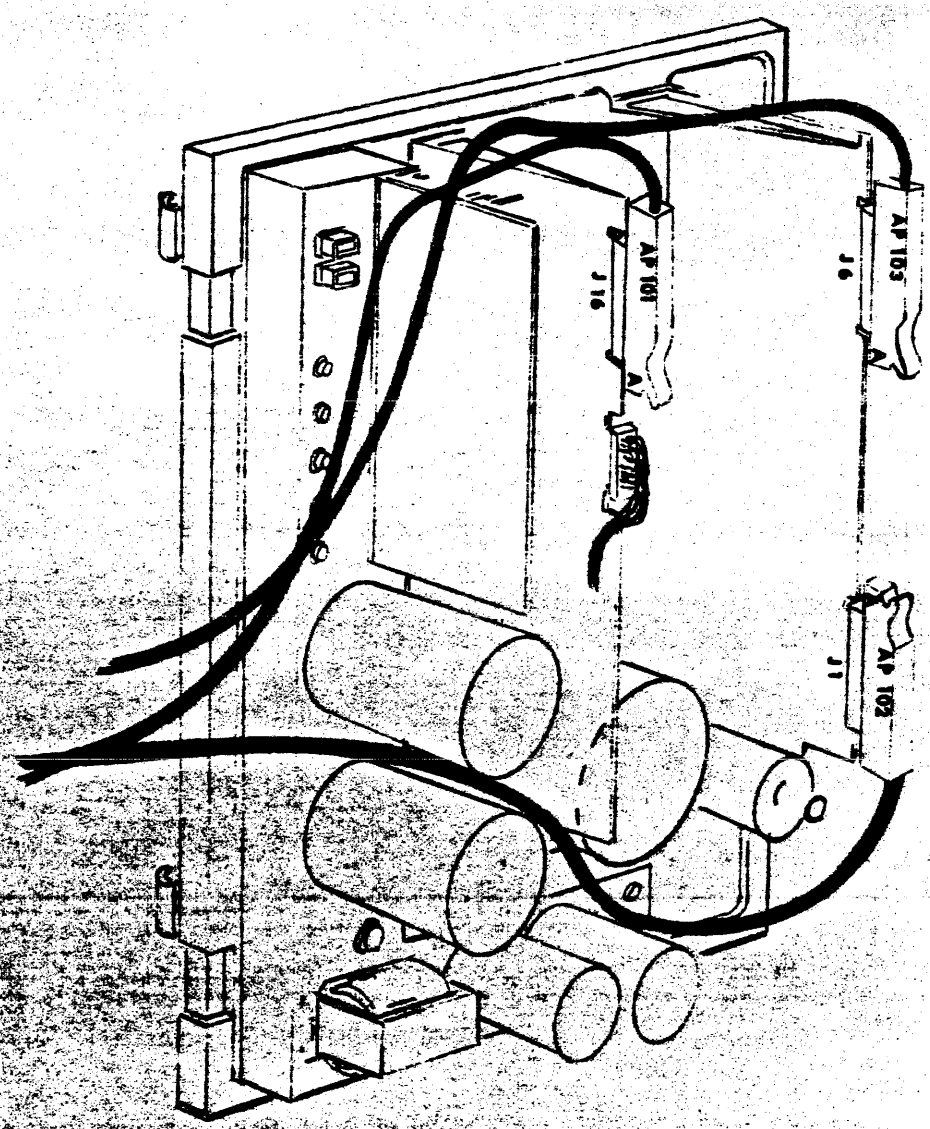


FIGURE 2
WANG NRZ TRANSPORT
INTERFACE CABLE CONNECTIONS

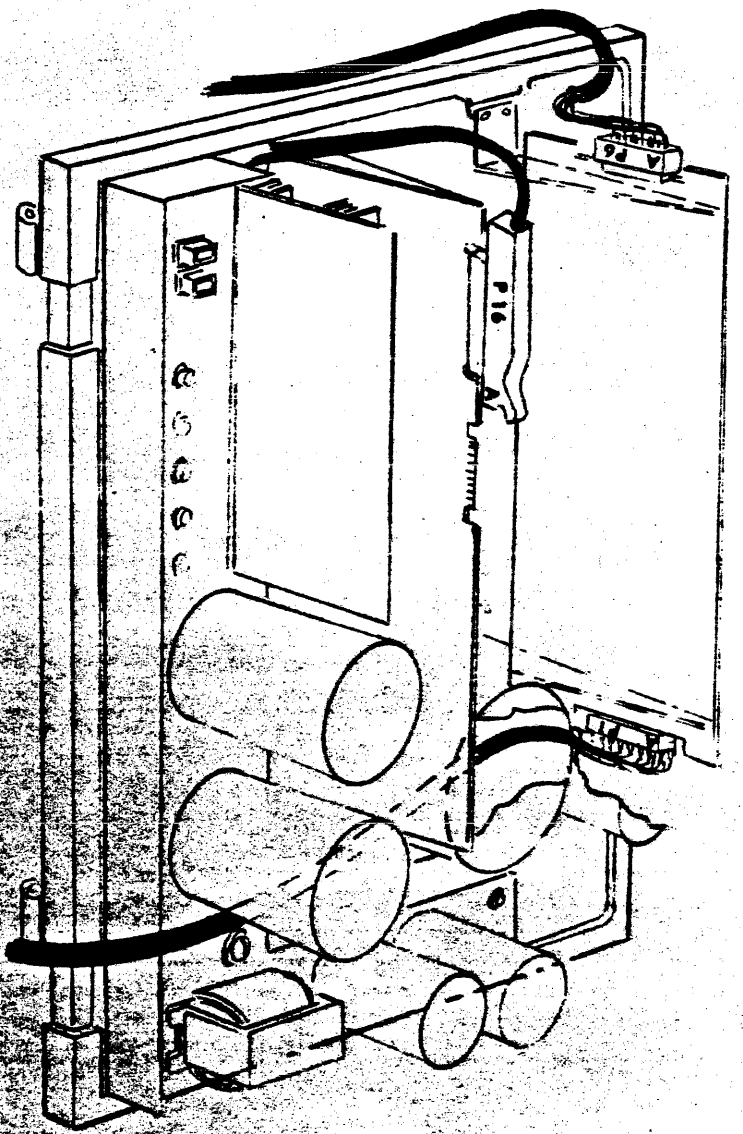


FIGURE 3
WANG PHASE ENCODED
TAPE TRANSPORT
CABLE CONNECTIONS

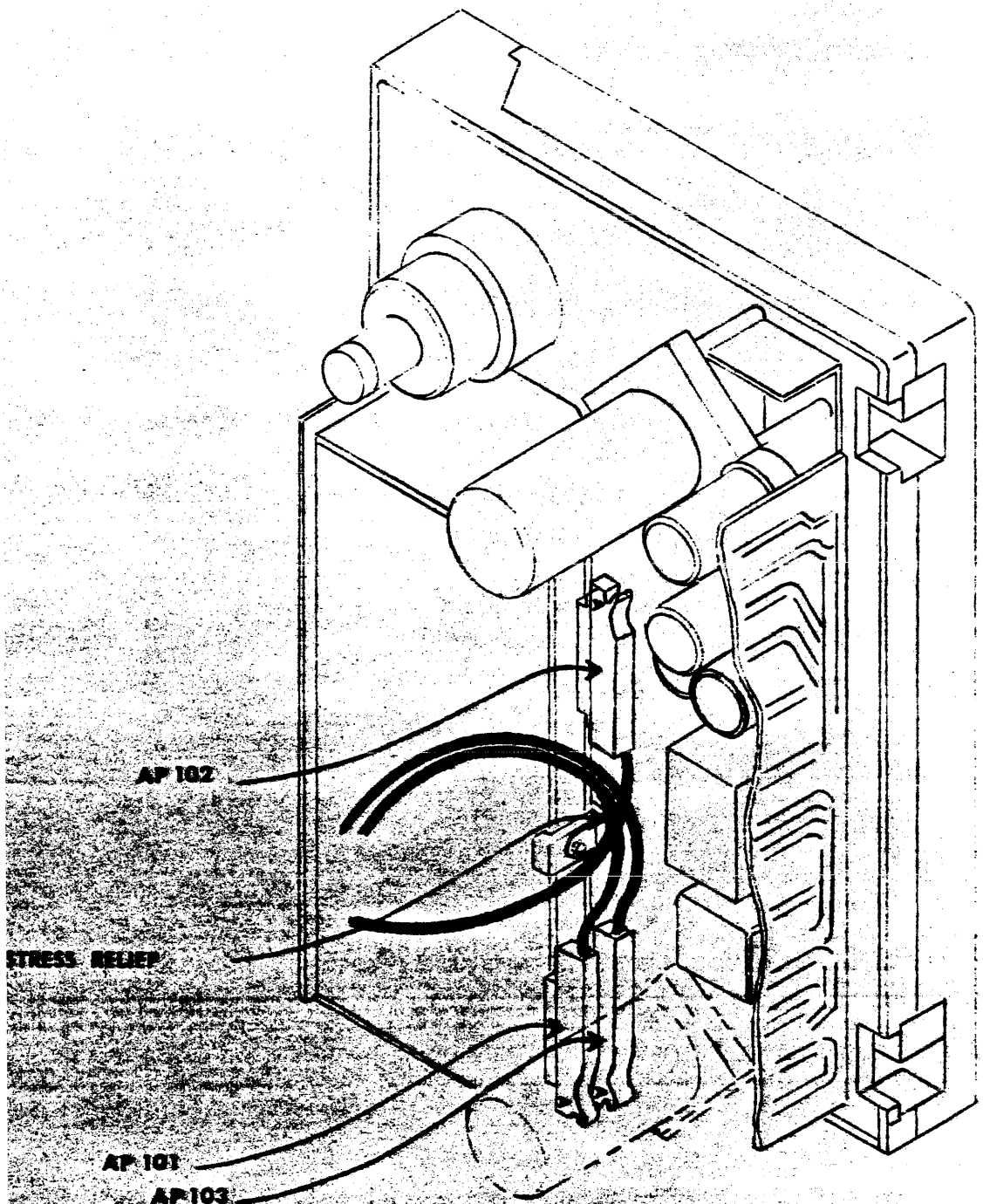


FIGURE 4
PERTEC NRZ & P.E. TRANSPORT
INTERFACE CABLE CONNECTIONS

SECTION I

GENERAL DESCRIPTION AND SPECIFICATIONS

1.1 FUNCTIONAL DESCRIPTION

The DATUM 1600 Phase Encoded (PE) Formatter provides the capability of writing and reading IBM-compatible or USASCII-compatible 9-track, phase-encoded, 1600 bits per inch magnetic tapes.

The 1600 PE Formatter provides a simplified computer-oriented interface to minimize the task of interfacing to a digital computer. All major operations are performed automatically under control of the Formatter.

Individual selection and operation of up to four "Daisy Chained" tape transports is permitted.

The transports can be a mixture of any two tape speeds, with Read/Write (single-stack head) or Read-After-Write (dual-stack head) inter-mixes permitted.

Tape transport motion control, Preamble and Postamble generation, error correction, inter-record gap generation and status reporting are included. Also provided are automatic recording of PE identification burst at BOT and checking for PE identification burst when reading from BOT. All write clocks and delay times are derived from a crystal-controlled oscillator. No "one shots" or RC delays are used.

The 1600 PE Formatter offers a selection capability such that two formatters (NRZI or 1600 PE) can be "Daisy Chained" to one computer adapter. This feature permits the mixing of 9-track, 1600-CPI, phase-encoded tape units; 9-track, 800-BPI and 7-track, 800/556/200 BPI tape units. It makes possible the control of up to eight tape units using only one computer adapter.

Card space and adequate +5-volt power is available for the computer adapter (may be wire-wrapped) in the Formatter.

The 1600 PE Formatter permits "On-the-fly" operation (continuous read or write at maximum tape speed without stopping in each inter-record gap). It writes the IBM- or USASCII-compatible file mark and recognizes file marks. It provides for the "Edit" feature (allows a record anywhere on a previously recorded tape to be replaced with an updated record).

There are no calibration or adjustment potentiometers in the Formatter. All timing is derived from a crystal oscillator.

The 1600 PE Formatter is compatible to the entire 12.5- to 112.5-ips tape-speed range without changing crystals. Field-changeable jumpers select the frequencies needed for the tape speed.

A special low-threshold data-recovery feature is provided.

Controls and indicators are provided to allow:

1. Switchable assignment of any tape unit number (0, 1, 2 or 3) to any of the four tape units (A, B, C, D).
2. Lamp indication of Formatter selection.
3. Lamp indication of tape unit selection.
4. Power on/off.

1.2 PHYSICAL DESCRIPTION

The DATUM Model 5091 1600 PE Formatter is designed to be mounted in a standard 19" EIA rack. The Formatter front panel is 5.25" high. The unit is 21" deep, with an additional allowance necessary of 2" for input/output cable service loop. Top and bottom covers may be easily removed for access to integrated circuits. Input/output cable connections are made at the rear of the Formatter via printed-circuit edge-connectors into which printed-circuit cable termination cards can be plugged.

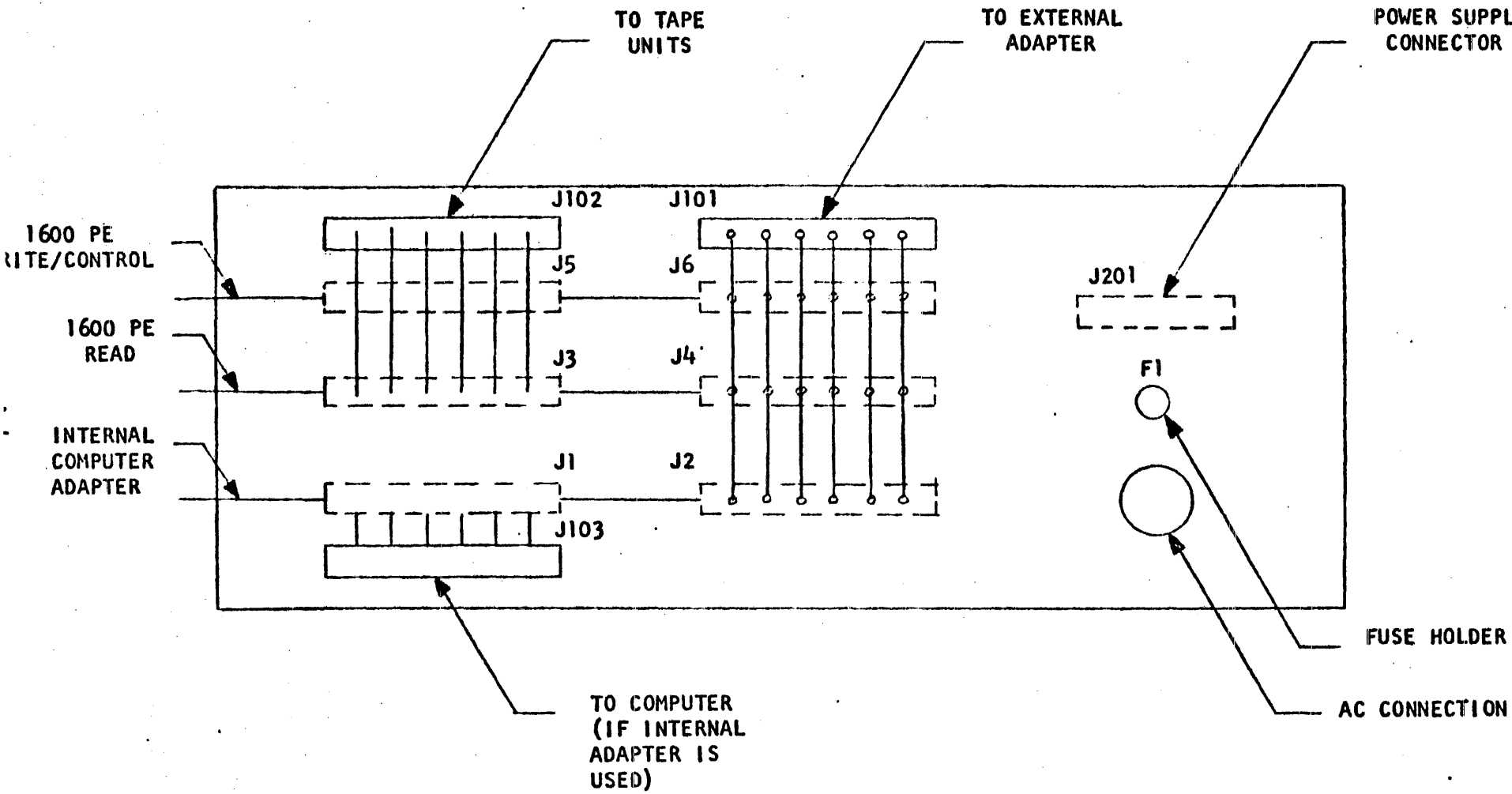


Figure 1-1. Rear View Formatter Connectors

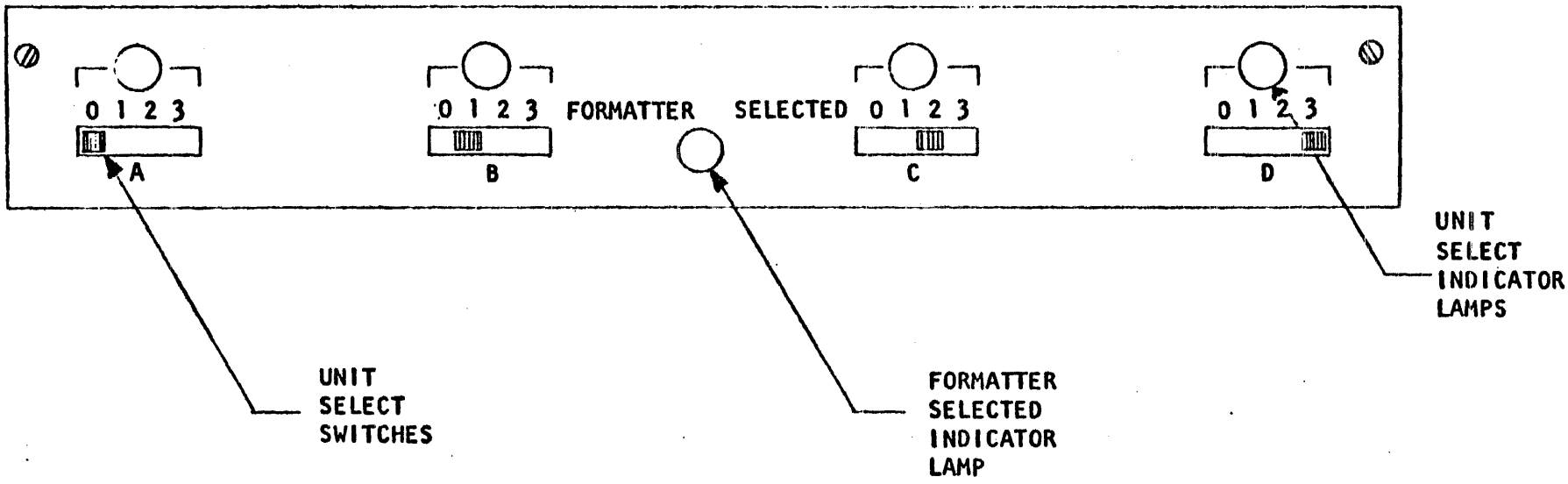


Figure 1-2. Front Panel

Power	115 VAC ±10% 230 VAC ±10% 160 watts maximum 48-400 Hz frequency
Circuits	All silicon
Operating Temperature	0° to 50°C
Storage Temperature	-40° to +70°C
Altitude	0 to 20,000 feet
Relative Humidity	10 to 95% (non-condensing)
Interface Voltages (DTL 900 series or TTL 7400 series compatible)	low = 0V ±.4V high = 3.9V ±1.5V

The interface is designed such that an open circuit is interpreted as a "high" signal.

Figure 1-3 illustrates the configuration for which the interface has been designed.

1.5 MAGNETIC TAPE FORMATS

Figure 1-4 illustrates the IBM and USASCII magnetic tape formats for 9-track phase-encoded tapes.

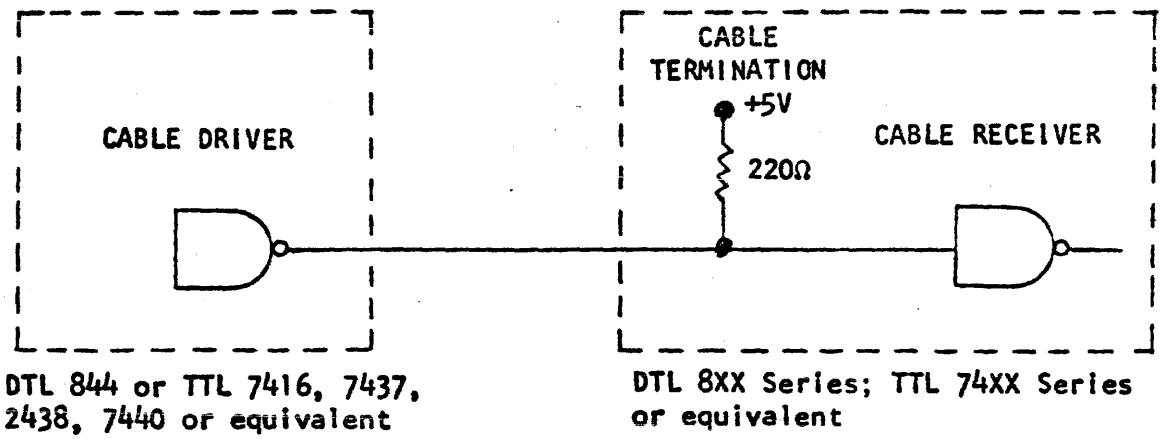
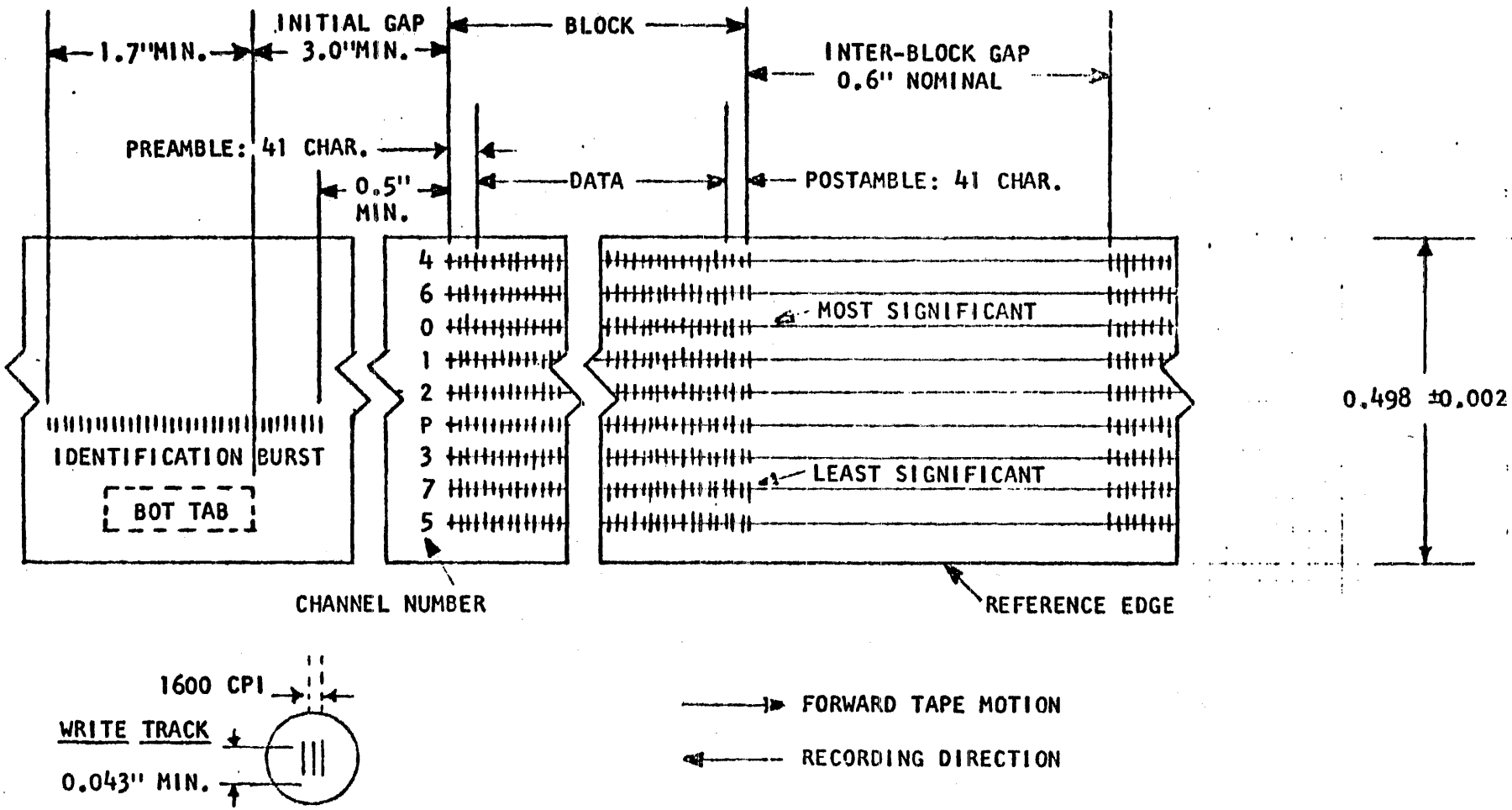


Figure 1-3. Interface Circuits



NOTES

1. Tape is shown with oxide side up.
2. Tape is to be fully saturated in the erased direction in the interblock gap and the initial gap.
3. The identification burst must extend past the end of the BOT marker.
4. All dimensions are given in inches.
5. There is a track placement tolerance of ±0.003 for each track.

Figure 1-4. PE Recording Format

SECTION II

INTERFACE

2.1 INTRODUCTION

Computer interface with the Formatter is provided at J101 for an external adapter or at J103 to the computer if the internal computer adapter is used. Tape unit interface is provided at J102. (See Figure 1-1, page 1-4.)

Datum printed circuit board #170189 is available for constructing the adapter internally. The P. C. Board can accept up to 196 14- or 16-pin wire-wrap sockets.

The interface connectors are 100-pin Amp 583485-3 printed circuit-edge connectors, which mate to DATUM part number 170192 cable terminator printed-circuit plug-in board.

Individual, 22-26 AWG, stranded, twisted-pair wires should be used. Maximum length should be 6' for the computer adapter interface and 20' (total) for the tape unit "Daisy Chain" bus. The twisted-pair should have at least one twist per inch and a minimum insulation thickness of .01 inch.

The ground wire of each twisted pair should be connected to ground as close to the origin or destination of the signal as possible (within 6 inches maximum) to minimize ground-loop-current "crosstalk" effects.

The interfaces are listed in Tables 2-1 and 2-2. The terms with a "bar" over them are "low" (0V) when active and the terms without a bar are "high" (+5V) when active.

selected transport to the write or read mode. This mode is maintained until the next SFC or SRC command is initiated.

The write mode within the transport is also switched to read mode if:

a) A RWC or OFC command is received.

b) Loss of interlock occurs.

c) The transport is manually switched offline.

$\overline{\text{OVW}}$ - Over Write. This signal is a level which causes the transport write current enable/disable to "ramp" on and off to minimize rate of change of recorded inter block gap magnetism when rewriting a record in the EDIT mode.

This signal level also causes the write current and DC erase head current to be turned off immediately after rewriting the new record (to keep from erasing the beginning of the next record).

$\overline{\text{RTH1}}$ - Read Threshold 1. This level selects a high threshold for marginal checking of written records when utilizing a single stack head. This is usually accomplished by backspacing over a newly written record and then reading forward in the high threshold mode to perform a parity check.

$\overline{\text{RTH2}}$ - Read Threshold 2. This level selects an extra low threshold for recovery of very low quality signals (on transports so equipped).

$\overline{\text{WARS}}$ - Write Amplifiers Reset. This signal controls the early turn off of write and erase currents after rewriting a record in the EDIT mode.

The negative going transition of this signal initiates the write current turn off. In NRZI transports, this signal also generates the LRC character.

$\overline{DDS}$ - Select high density. Low = select high density (for NRZI Formatter only) for 7 track transport.

2.2.1.3 Write Data

$\overline{WDS}$ - Write Data Strobe. This is a clock utilized to copy the write data ($\overline{WDP}$ and $\overline{WD0}$ through $\overline{WD7}$) in to the selected transport write flip-flops. The data levels must be static during $\overline{WDS}$ and the trailing edge (positive going) of $\overline{WDS}$ is used to clock the flip-flops. The clock rate is twice the character rate for 1600 CPI and at the character rate for NRZI.

$\overline{WDP}$, $\overline{WD0}$ through $\overline{WD7}$ - Write data. $\overline{WDP}$ is the odd parity bit, $\overline{WD0}$ is the most significant bit, and $\overline{WD7}$ is the least significant bit. $\overline{WD0}$ and $\overline{WD1}$ are not used for 7 track NRZI operation.

These signals are presented to the selected transport along with the $\overline{WDS}$ clock. For the 1600 CPI Formatter, the first negative going transition (in writing a record) is the "zero bit" of the preamble. The write data is presented in phase encoded form. For the NRZI Formatter, the write data is presented in logic level form (low = logic 1, high = logic 0).

2.2.2 Transport to Formatter

2.2.2.1 Status lines.

$\overline{RDY}$ - Ready. A level that is low only when the selected transport is:

a) Interlocked.

b) Through the initial load or rewind to load point sequence.

c) On line.

d) Not rewinding.

Note: A transport will go NOT Ready for approximately .5 second after reversing into load point and does not go Ready until approximately .5 second after termination of a Rewind.

$\overline{ONL}$ - On line. A level that is low when the selected transport is manually switched on line (to place it under remote control).

$\overline{RWD}$ - Rewinding. A level which is low while the selected transport is rewinding. The level remains low until the transport completes the automatic "return to load point" sequence but the transport does not become Ready until approximately .5 second after the $\overline{RWD}$ signal terminates.

$\overline{FPT}$ - File Protect. A level which is low when the selected transport has a supply reel of tape mounted which does not have a write enable ring installed.

$\overline{LDP}$ - Load Point. A level which is low when the selected transport's beginning of tape reflector is located under the photo sensor, interlocks are made, and the initial load or rewind sequence is completed.

$\overline{EOT}$ - End of Tape. A level which is low when the end of tape reflector is under the photo sensor in the selected transport. This signal is not staticised and neither the positive or negative going transition is "clean".

$\overline{NRZ}$/PE - Non Return to Zero/Phase Encoded. A level which reports the selected transport type. Low for NRZ type, High for PE type.

$\overline{SINGLE}$/DUAL - Head Stack. A level which reports the selected transport head type. Low for single stack, High for dual stack "read while writing".

$\overline{Low}$/High - Transport Speed. A level which reports the selected transport tape motion speed.

Low = low speed
High = high speed

$\overline{7\ TRK}$/9 TRK - Transport Type.

Low = 7 track

High = 9 track

$\overline{DDI}$ - Data Density Indicator

Low = High Density Selected

High = Low Density Selected

2.2.2.2 Read Data & Read Clock

$\overline{RDP}$, $\overline{RD0}$ through $\overline{RD7}$ - Read Data.

a) 1600 CPI Formatter:
Read Data from the selected transport is identical to the Write data wave forms supplied to the transport. There is no read strobe.

The Phase Encoded signals are high during an Inter Block Gap or when the tape is not in motion. In the forward direction the first negative going transition is the zero bit of a preamble. In the reverse direction the first negative going transition is the last "phase" transition of the postamble hence the zero bit transition will be a positive going transition in read reverse.

b) NRZI Formatter:
Read Data is in logic level form (low = logic 1, high = logic 0) and is presented along with a negative going read strobe ($\overline{RDS}$).

2.3 FORMATTER/COMPUTER ADAPTOR INTERFACE

2.3.1 General

Table 2-2 lists the signals and pins for the Formatter/computer adaptor interface.

All signals from the Formatter to the Computer Adaptor may be "daisy chained" to a second Formatter such that one of the two Formatters may be addressed to operate with the Computer Adaptor. In order to accomplish this, all such signals are "low active" open collector cable driver integrated circuits capable of sinking 25 ma. This allows all such signals to be terminated with resistors to +5V at the Computer Adaptor.

2.3.2 Formatter to Computer Adaptor

2.3.2.1 Status

Most of the status signals are generated by latch flip-flops that retain the occurrence of the status until the next command is accepted by the Formatter (or the Formatter is deselected).

Some of the status signals are levels from the Formatter or from the selected transport that are gated with the Formatter address line hence are not reset by the command clock. These status signals are marked by note 1 in Table 2.

$\overline{\text{EOTS}}$ - End of Tape Staticised. When low, the $\overline{\text{EOTS}}$ level indicates selected tape transport is on or has passed over (in the forward direction) the EOT reflective tab. The $\overline{\text{EOTS}}$ signal remains low until a "reverse direction" command (such as rewind, backspace or read reverse) is accepted by the Formatter. Thus the program only need check for $\overline{\text{EOT}}$ after completion of writing each record.

$\overline{\text{EOTS}}$ is also reset by power on, or the EXT RESET signal from the Computer Adaptor.

$\overline{\text{REJECT}}$ - Rejected Command Status. Goes low when the command accompanying the command clock (STROBEC) is rejected by the Formatter.

Table 2-2. Formatter/Computer Adaptor Interface

J101/J2 Pins	Formatter to Computer Adaptor			J101/J2 Pins	Computer Adaptor to Formatter	
59		$\overline{\text{EOTS}}$		71	$\overline{\text{FADI}}$	
80		$\overline{\text{REJECT}}$		91	S1	Addressing
73	1) 2)	$\overline{\text{9 TRK}}$		84	S2	
24	1)	$\overline{\text{NRZ}}$				
22	1)	$\overline{\text{SINGLE}}$		5	STROBEC	Command Clock
20	1)	$\overline{\text{LOW}}$				
87		$\overline{\text{TMER}}$		92	EXT RJCT	
93		$\overline{\text{PARITY ER}}$	Status	90	SET REV	
70		$\overline{\text{FM}}$		32	SET WCC	
95	1)	$\overline{\text{RDY}}$		55	SET WFM	
9	1)	$\overline{\text{RWDG}}$		57	SET GAP	Commands
43	1)	$\overline{\text{FPT}}$		89	SET FSR	
47	1)	$\overline{\text{LDP}}$		58	SET RCC	
31		$\overline{\text{WCC}}$		64	SET CLR	
38		$\overline{\text{RCC}}$		68	SET REW	
41	4)	$\overline{\text{IDENTS}}$		61	SET OFL	
40	4)	$\overline{\text{CERS}}$				
				66	3) $\overline{\text{GEN ODD PARITY}}$	
19		$\overline{\text{RP}}$		77	3) $\overline{\text{HI DENSITY}}$	
15		$\overline{\text{R0}}$		6	$\overline{\text{THR1}}$	
26		$\overline{\text{R1}}$		8	$\overline{\text{THR2}}$	Modes
17		$\overline{\text{R2}}$		85	$\overline{\text{EDIT}}$	
25		$\overline{\text{R3}}$	Read Data	63	1) TRD	
11		$\overline{\text{R4}}$	& Clock	75	$\overline{\text{STOP SPACE}}$	
30		$\overline{\text{R5}}$		29	3) $\overline{\text{CD}}$	
13		$\overline{\text{R6}}$				
28		$\overline{\text{R7}}$		37	$\overline{\text{B0}}$	
21		$\overline{\text{RSTROBE}}$		62	$\overline{\text{B1}}$	
				39	$\overline{\text{B2}}$	
94		$\overline{\text{CBUSY}}$		42	$\overline{\text{B3}}$	
65		$\overline{\text{DBY}}$		45	$\overline{\text{B4}}$	Write Data
78		$\overline{\text{RCAS}}$		52	$\overline{\text{B5}}$	
82		$\overline{\text{DATA FLAG}}$	5)	46	$\overline{\text{B6}}$	
69		$\overline{\text{WRMSB}}$	6)	49	$\overline{\text{B7}}$	
76		$\overline{\text{RJCT}}$	Reject Pulse			
79		$\overline{\text{CK WD CNT}}$	7)	7	$\overline{\text{W/R ACK}}$	Data Transfer Acknowledge.
34		$\overline{\text{CLK}}$	Clock	72	HALT	Last Word Transferred.
88		$\overline{\text{WRP}}$	Write Clock Precede	67	$\overline{\text{EXT RESET}}$	
		Total = 36			Total = 33	

1) Status levels not reset by acceptance of new command.
2) Always 1 when 1600 Formatter is addressed.
3) Not used by 1600 Formatter.
4) Always 0 (open circuit) from NRZI Formatter.
5) Data Transfer Flag.
6) Write Most Significant Byte.
7) Check Word Count Pulse.

The reject status is needed to keep the computer program from "hanging up" when it issues a command that the Formatter can't perform. Normally the computer adaptor is designed to interrupt the program when the commanded function terminates (based on the Formatter returning to the NOT busy state). If the Formatter can't perform the commanded function, the $\overline{\text{RJCT}}$ pulse can be utilized to set the interrupt. When interrupted, the $\overline{\text{REJECT}}$ status line can be inspected by the program (before going on to the next function) to ascertain if the command was accepted.

The following conditions cause a reject:

a) Formatter busy with transport motion or selected transport busy and any command other than a clear is issued.
b) Reverse motion command issued while at BOT.
c) Write command issued while no write ring is installed on selected transport.
d) Any "external reject" condition exists in the computer adaptor (a typical use is detection of a non-valid command code).

$\overline{\text{9 TRK}}$ - Nine Track Tape Transport Selected. Available only if tape unit is equipped to supply this status.

Low = 9 track transport is selected.
High = 7 track transport is selected.

$\overline{\text{NRZ}}$ - Non Return to Zero Tape Transport Selected. Available only if tape unit is equipped to supply this status.

Low = NRZI transport selected.
High = 1600 PE transport selected.

$\overline{\text{SINGLE}}$ - Single Gap Head Transport Selected. Available only if tape unit is equipped to supply this status.

Low = Single Gap Head (Read/Write).
High = Dual Gap Head (Read while writing).

$\overline{\text{LOW}}$ - Low Speed Tape Unit Selected. Available only if tape unit is equipped to supply this status.

Low = Low Speed.

High = High Speed.

$\overline{\text{TMER}}$ - Data Transfer Timing Error Status.

Low = Error.

High = No Error.

Level that indicates detection of computer adaptor failure to transfer a character before the next character transfer is required. This check is performed both in write and read modes.

$\overline{\text{Parity ER}}$ - Parity Error Status.

Low = Error

Level that indicates error condition was detected on last operation.

a) 1600 CPI Formatter:

1. Correctable error occurred (CERS will be low also).
2. Uncorrectable error occurred (CERS will be high).
3. False preamble or postamble was detected.
4. Skew error.
5. Multi track dropout.

For an error condition consisting of a vertical parity error <u>without</u> a corresponding single track dropout the $\overline{\text{PARITY/ER}}$ line will be pulsed low during Read Clock (RSTROBE) time to tag the character in question.

b) NRZI Formatter:

1. LRC error occurred.
2. VRC error occurred.

$\overline{\text{FM}}$ - File Mark Status.

Low = File mark detected.

High = No file mark detected.

$\overline{\text{RDY}}$ - Ready Status.

Low = Selected transport is ready.

High = Selected transport is not ready.

$\overline{\text{RWDG}}$ - Rewinding Status.

Low = The selected transport is rewinding or is not ready yet after a rewind.

High = The selected transport is not rewinding.

The $\overline{\text{RWDG}}$ status flip-flop doesn't indicate termination of rewind until the transport also indicates READY (if a single transport is commanded to rewind and the Formatter waits until the rewind terminates). In multiple transport systems it is possible to initiate rewind on one transport, select and operate another transport, and then re-select the first transport and find that it is not reporting the rewinding condition, yet isn't ready (because it stays not ready for approximately .5 second after termination of rewind). For this reason, the computer program should always check for ready status as well as "done rewinding" before proceeding after any rewind on multiple tape systems.

$\overline{\text{FPT}}$ - File Protect Status.

Low = Selected transport is protected against writing (no write ring installed on supply reel).

High = Writing is enabled.

$\overline{\text{LDP}}$ - Load Point (see $\overline{\text{LDP}}$ under section 2.2.2.1)

Low = Selected transport is at BOT.

High = Not at BOT.

$\overline{\text{WCC}}$ - Write Mode. Level that indicates when the Formatter is writing a record.

Low = Writing.

High = Not writing.

Typically used with "unpack" signal $\overline{\text{WRMSB}}$ to control the computer data requests and computer adaptor to Formatter write strobes ($\overline{\text{W/R ACK}}$) when unpacking a computer word into two tape characters.

$\overline{\text{RCC}}$ - Read Mode. Level that indicates the Formatter is performing a read operation.

Low = Reading

High = Not reading

Typically used to indicate "data transfer direction" to the computer and to disable detection of read mode record length error logic (on the computer adaptor) when not reading. Also disables the read mode control of the computer adaptor data transfer control logic even though read strobes are received for "read while write" operations.

$\overline{\text{IDENTS}}$ - 1600 CPI Identification Status.

Low = 1600 CPI tape identified at BOT.

Signals detection of 1600 CPI "Burst" when selected tape is commanded to move off BOT. (1600 CPI Formatter only)

$\overline{\text{CERS}}$ - Corrected Error Status.

Low = Single track error was corrected by the 1600 Formatter in the last record. Always logic 0 (open circuit) from NRZI Formatter.

2.3.2.2 Read Data & Clock

The read data is completely "buffered" in a special register (supplied on the Formatter) such that no external register in the computer adaptor is required. The data is allowed to change just before the leading edge of the read strobe pulse ($\overline{\text{RSTROBE}}$) and is static throughout $\overline{\text{RSTROBE}}$ and until the leading edge of the next $\overline{\text{RSTROBE}}$ pulse.

The $\overline{\text{RSTROBE}}$ pulse actually isn't needed for simple 8 bit single character interfaces to computers but is included to allow more sophisticated computer adaptors to be built which "pack" successive pairs of tape character into a 16 bit word for computer entry. In this case, at least 8 bits must be stored on the computer adaptor.

The $\overline{\text{DATA FLAG}}$ Control signal goes low at the trailing edge of the $\overline{\text{RSTROBE}}$ pulse to signal that read data is ready for output from the Formatter. The computer adaptor must respond with $\overline{\text{W/R ACK}}$ before the next RSTROBE pulse occurs or the data transfer timing error ($\overline{\text{TMER}}$) will latch.

$\overline{\text{RSTROBE}}$ - Read Strobe Clock. Negative going pulse that can be utilized to clock the levels present on the data lines into an external register. Normally also used by the computer adaptor to detect read record lengths that are longer than expected by gating with a signal that indicates all the characters asked for by the computer program have been input. If more $\overline{\text{RSTROBE}}$'s occur, after this signal indicates that the record length asked for has been input, then the record is longer than expected.

2.2.2.3 Control

$\overline{\text{CBUSY}}$ - Controller Busy.

Low = Controller busy.

High = Controller not busy.

Goes low at the leading edge of the STROBEC command clock when a new command is accepted and remains low until the operation has finished and all tape motion has ceased.

The offline command does not cause the controller to go to the busy state and the rewind command can be jumper selected to not cause the controller to go to the busy state.

The computer adaptor normally makes use of $\overline{\text{CBUSY}}$ to inhibit new commands. However, for continuing with writing or reading "on-the-fly", the computer adaptor logic can ignore the $\overline{\text{CBUSY}}$ level and initiate the next command when the $\overline{\text{DBY}}$ (data busy) signal terminates at the beginning of the IRG (inter-record gap).

$\overline{DBY}$ - Data Busy

Low = Data write or read portion of operation is in process.

The $\overline{DBY}$ does not occur for offline, rewind, or clear & select type commands.

The $\overline{DBY}$ signal begins after the initial "Up to Speed" delay transpires and remains low until the motion command line (SFC or SRC) to the selected transport is terminated. At this time the transport begins deceleration to stop in the inter-record gap. If continuous "on-the-fly" operation is desired (to halve the amount of time required to traverse the IRG) then the computer adaptor can initiate the next command immediately after $\overline{DBY}$ terminates rather than waiting until $\overline{CBUSY}$ terminates. The only restrictions are that the next command must be the same type and direction as the preceding command.

The computer adaptor is usually designed to notify the computer program when $\overline{DBY}$ terminates and it is left up to the computer program to read status (to determine if the last command terminated correctly, check that the new command is of the same type and direction as the old, and issue the new command).

Commands are "typed" as to whether they are read or write commands as follows:

Command Types

Read	Write
Space Forward	Erase 3" Gap
Space Reverse	Write File Mark
Read Record Forward	Write 1 Record
Read Record Reverse	
Test Read Forward	

$\overline{\text{RCAS}}$ - Read Clock Activity Sensor. Used in NRZI Formatter to separate the CRC/LRC characters from the data character in a read forward operation. In NRZI Formatter, low = data portion of record. In read reverse operations, $\overline{\text{RCAS}}$ does not separate the CRC/LRC characters from the data hence the program must expect one or two more characters to be input than in the read forward mode and must discard the CRC/LRC characters. This may be done for the 9 track case by setting the record length to two characters more than in the forward mode. Since the CRCC may be all zero, program would have to test the record length error status to find out whether to discard: 1. The first character only (LRCC) if record is too short. 2. The first two characters (LRCC & CRCC) when the record is the expected two characters longer than in the forward mode. In the 7 track case the record length must be set to one extra character (only LRCC is generated for 7 track) and the record length error status inspected to determine whether to discard the first character or not. If the record is the expected one character longer, the first character (LRCC) must be discarded. If the record indicates that it is too short, then the LRC character must have been zero hence the first character is data and should be retained.

For 1600 CPI Formatter, the $\overline{\text{RCAS}}$ signal is switched low throughout each data record in both the forward and reverse read operations.

$\overline{\text{DATA}}$ $\overline{\text{FLAG}}$ - Data Transfer Request Flag.

Low = transfer request active.

The data flag is utilized for <u>both</u> write and read functions. It is cleared by the leading edge of the $\overline{\text{W/R ACK}}$ pulse from the computer adaptor.

In the case of writing, the data flag is set one character time before the character is needed hence the amount of time allowed before the $\overline{\text{W/R ACK}}$ pulse must be received is dependent solely upon the tape speed. If the $\overline{\text{W/R ACK}}$ pulse is not recieved in time, the $\overline{\text{TMER}}$ (data transfer error)

In the case of reading, the data flag is set at the trailing edge of the read strobe ($\overline{\text{RSTROBE}}$) pulse. Due to tape speed variations and bit crowding effects, the worst case time allowed may be as short as one-half the character time but is also directly dependent upon the tape speed. If the $\overline{\text{W/R ACK}}$ pulse is not received before the next $\overline{\text{RSTROBE}}$ is generated then the $\overline{\text{TMER}}$ latch is set.

$\overline{\text{WRMSB}}$ - Write Most Significant Byte.

Low = Odd characters

High = Even characters

Flip-flop that toggles to the opposite state for each character to be written on tape to allow 16 bit computer words to be easily "unpacked" into two 8 bit tape characters by the computer adaptor.

Not needed for simple 8 bit transfer modes of operation.

$\overline{\text{WRMSB}}$ is switched shortly before $\overline{\text{DATA FLAG}}$ is set and is static throughout $\overline{\text{DATA FLAG}}$ time hence can be gated with $\overline{\text{DATA FLAG}}$ to determine whether to set the computer data request flag or to generate the $\overline{\text{W/R ACK}}$ signal back to the Formatter when "unpacking".

$\overline{\text{RJCT}}$ - Reject Pulse. Negative going pulse which sets the $\overline{\text{REJECT}}$ status flip-flop.

This pulse can be utilized by the computer adaptor to trigger the interrupt normally set by the $\overline{\text{DBY}}$ or $\overline{\text{CBUSY}}$ termination.

The computer program should always check status after a command operation signals completion to determine if the command was accepted & performed correctly or if the command was rejected.

$\overline{\text{CK WD CNT}}$ - Check Word Count Pulse. Negative going pulse at the end of each record which is usually used by the computer adaptor to

set a "record length error" status bit if the record read is shorter than expected.

Usually gated with signal in computer adaptor that signifies that the record length expected by the computer program has been input. If this signal isn't set when $\overline{\text{CK WD CNT}}$ pulse occurs then the record must have been shorter than expected.

$\overline{\text{CLK}}$ - Clock. Clock derived from crystal oscillator on formatter.

$\overline{\text{WRP}}$ - Write Pulse Precede. Pulse that precedes write flag (DATA FLAG) which may be utilized to test for data transfer complete before the next one is initiated.

2.3.3 Computer Adaptor to Formatter

General

The computer adaptor driver circuits to the Formatter should be capable of sinking 30 milliamps when at the low level. They need not supply any current when at the high level since resistor termination's to +5V are supplied within the Formatter. The drivers are not required to be "open collector" types however (since no "wired or" function is utilized).

2.3.3.1 Addressing

$\overline{\text{FAD1}}$ - Formatter Address

Low = Formatter #1 addressed.

High = Formatter #Ø addressed.

This level must remain static throughout execution of any command. The Formatters have capability of jumper specifying whether their address is Ø or 1.

S1, S2 - Transport Select Address Lines. These levels are decoded by the Formatter to select one of the four transports. The levels must remain static throughout any operations except Rewind. A transport can be commanded to rewind and a different transport selected immediately.

S1	S2	Tape Unit Selected
Low	Low	0
High	Low	1
Low	High	2
High	High	3

2.3.3.2 Commands & Command Clock

General

The commands are stored in the Formatter by the command clock pulse if the command is not "rejected" by the Formatter.

$\overline{\text{CBUSY}}$ is set at the trailing edge of the command if the command is accepted. When the $\overline{\text{CBUSY}}$ signal terminates, the operation has been completed by the Formatter and the Formatter is ready to accept another command.

Commands - The offline command never causes $\overline{\text{CBUSY}}$ to set and $\overline{\text{CBUSY}}$ set upon rewind command acceptance is jumper selectable.

The command signals must be static from 100 nanoseconds before the leading edge to 100 nanoseconds after the trailing edge of the command clock.

Table 2-3. illustrates the valid Formatter functions and the corresponding command lines that are required to be "high" in order to

initiate the associated function. All other command lines must be "low" with the exception of EXT RJCT which over-rides all other commands.

Command Clock. The command clock (STROBEC) must be a positive going pulse of 100 nanaseconds (or more) pulse width.

Table 2-3. Commands

Formatter Function	Command Signals "High"
1) Write File Mark	SET WFM
Erase 3" Gap then Write File Mark	SET WFM/SET GAP
1) Write Record	SET WCC
Erase 3" Gap then Write Record	SET WCC/SET GAP
2) 3) Space Forward	SET FSR
1) 2) 3) Space Reverse	SET REV
3) 4) Read Forward	SET RCC
3) Read Reverse	SET RCC/SET REV
Erase 3" Gap	SET GAP
Reject	5) EXT RJCT
Clear	SET CLR
Rewind	SET REW
Offline	SET OFL
Rewind and then go offline	SET REW/SET OFL

5) overrides all other commands.
4) can be in either normal or test read mode.
3) can be read in various read threshold modes.
2) can be multiple record spacing under control of STOP SPACE mode.
NOTES: 1) can be in edit or normal modes.

2.3.3.3 Modes

The mode lines are levels which are <u>not</u> stored in the Formatter by the command clock hence must be stored by the computer adapter. They

must all remain static (with the exception of STOP SPACE) throughout execution of a command by the Formatter.

GEN ODD PARITY - Generate Odd Parity. This line is ignored by the 1600 CPI Formatter. The NRZI Formatter uses it to control parity generation for 7 track tapes (if in the REMOTE parity control mode). Low = even parity, high = odd parity.

$\overline{\text{HI DENSITY}}$ - Select High Density Write Mode. The 1600 CPI Formatter ignores this line. The NRZI Formatter utilizes the line to control High/Low write density selection for 7 track tape transports (if in the REMOTE density select mode) high = low density, low = high density.

$\overline{\text{THR1}}$ - Select Read Threshold One. Used for single track head transports to enable a marginal read amplitude check to be made immediately after writing each record (by backspacing then reading forward) to determine whether that section of tape should be erased and the record re-written further down the tape.

Low = Marginal threshold (high threshold).
High = Normal threshold.

$\overline{\text{THR2}}$ - Select Read Threshold Two. Used for transports equipped with the extra low read threshold capability for recovery of low amplitude data.

Low = Extra low threshold.
High = Normal threshold.

$\overline{\text{EDIT}}$ - Edit Mode. Enables records to be replaced with equal length records anywhere on a tape.

Low = Edit mode.
High = Normal mode.

The record to be replaced must first be backspaced over in the edit mode (to position the write head correctly) then rewritten in the edit mode (to cause the erase head and write current to be turned off

immediately at the end of the record before the erase head erases into the following record).

$\overline{TRD}$ - Test Read Mode.

Low = Normal mode.

High = Test read mode.

The NRZI Formatter utilizes the line to control access to the CRC/LRC characters (when reading forward) for diagnostic and maintenance purposes. In test read mode, the data flag is allowed to trigger for the CRC/LRC characters. The 1600 Formatter allows access to the postamble characters (or to characters following postamble detection in cases of false postamble detection).

STOP SPACE - Stop Forward of Backspacing.

High = Normal (Formatter spaces 1 record for each command).

Low = Continuous spacing.

The $\overline{RCAS}$ signal can be used by the computer adaptor to count the number of records spaced over to determine when to switch STOP SPACE high to terminate multiple record spacing. The leading edge of $\overline{RCAS}$ should be used to count records and switch STOP SPACE high upon detection of the last record to be spaced over.

$\overline{CD}$ - Core Dump Mode.

Low = Core dump mode.

High = Normal mode.

Ignored by 1600 CPI Formatters. The NRZI Formatter utilizes this line to operate 9 track tape machines in a 7 track mode where in 7 track type file marks are written and detected. This mode is necessary for compatibility with some computer systems in the field.

2.3.3.4 Write Data

The write data consists of eight lines which must be stable during the W/R ACK pulse transmitted from the computer adaptor to the Formatter. Odd parity is generated in the Formatter for recording.

A write data storage register is included in the Formatter so that none is required in the computer adaptor.

$\overline{B0}$ through $\overline{B7}$ are the write data lines. $\overline{B0}$ is the most significant bit. (low = logic 1, high = logic 0).

2.3.3.5 Control

$\overline{W/R\ ACK}$ - Write/Read Acknowledge. This negative going pulse is used to acknowledge the $\overline{DATA\ FLAG}$ request for data transfer in both read and write operations. The pulse must be at least 100 nanoseconds wide.

In the write operation the $\overline{W/R\ ACK}$ pulse is used to clock the levels present on the $\overline{B0}$ through $\overline{B7}$ lines into the Formatter write storage register and to reset the $\overline{DATA\ FLAG}$ flip-flop.

In the read operation the $\overline{W/R\ ACK}$ pulse is merely used to reset the $\overline{DATA\ FLAG}$ flip-flop.

The leading edge of the $\overline{W/R\ ACK}$ signal is delayed in the Formatter and utilized to reset the DATA FLAG flip-flop such that the Formatter $\overline{DATA\ FLAG}$ signal can <u>itself</u> be gated at alternate character times onto the $\overline{W/R\ ACK}$ line to reset itself (in "Pack/Unpack" modes of operation). This is useful since actual data transfers with the computer must take place only for every other tape character time yet the Formatter data transfer requests must be serviced for <u>every</u> 8 bit tape character (since it only provides storage for one 8 bit tape character).

Halt - Halt data transfer.

The signal is used to initiate termination of writing a record or to terminate data transfer requests ($\overline{DATA\ FLAG}$) from the Formatter when

reading a record. The signal is normally low and should go high after the last $\overline{\text{W/RACK}}$ pulse to signal termination of the record. Must remain high until the next command is issued.

In the write operation, the 1600 CPI postamble (or the NRZI CRC/LRC character) are written and a portion of the inter-record gap is erased before the tape transport begins to decelerate to halt in the IRG.

In the read operation, the Formatter continues on until the true end-of-record is detected before initiating the halt in IRG process.

$\overline{\text{EXT}}$ $\overline{\text{RESET}}$ - External Reset. The external reset line allows the Formatter to be cleared to initial conditions from such signals as the computer "start" button etc.

Low = Reset

High = Normal

SECTION III

THEORY OF OPERATION

3.1 INTRODUCTION

This section contains information on the operation of the Model 5091 1600 PE Magnetic Tape Formatter.

The information in this section is divided into two major sections. The first will be a discussion of the block diagram (Figure 3-1). This will provide an overall functional description and will illustrate the relationship between the Formatter, the tape transports, and the computer adapter. The second section is a discussion of the command execution, illustrated by timing diagrams. The section describes the operation of the Formatter circuitry during execution of computer-originated instructions.

3.1.1 Functions of the Formatter

The Formatter performs three basic functions. These are:

1. Control
2. Write
3. Read

The Formatter provides control over the selected tape unit including all timing necessary to perform automatically all write, read, rewind, space forward, space backward and rewind commands. Upon completion of the commanded operation, status is provided so that the computer can ascertain whether the operation was performed correctly.

The Formatter performs all the write functions for erasing tape, writing a file mark or writing a record of data. The phase mode identification burst is automatically recorded before the first record when

1600 CPI TAPE UNITS

1600 CPI FORMATTER

COMPUTER ADAPTER

SLCT 0, 1, 2, 3

SFC
SRC
RWC
OFC
SWS
DVW
RTN1
RTN2
WAB
BTLL

WDS

WDP, 0 → 7
WRITE DATA

RDP, RD0 → RD7
READ DATA

RDY
ORL
RWD
FPT
LDP
EOT
NRZ/PE
SINGLE/DUAL HEAD
LOW/HIGH SPEED

STATUS

RJCT

FADI

STROBEC
EXT RJCT, SET REV, SET WCC, SET WFM, SET GAP, SET FSR, SET RCC, SET CLR, SET REV, SET OFL

RJCT

S1, S2

THR1, THR2, EDIT, STOP SPACE

DATA FLAG
WRMSB
WR ACK
HALT

CK WD CNT

RCAS

BO THROUGH B7

CBUSY, DBY

EXT RESET

RSTROBE

RP, R0 THROUGH R7

EOTS, REJECT, 9TRK, NRZ/PE SINGLE/DUAL HEAD, LOW/HIGH SPEED, TMER, PARITY ER, FM, RDY, RWDG, FPT, LDP, WCC, RCC IDENTS, CERS

WRITE CLOCK
SPEED CLOCK
CRYSTAL OSCILLATOR AND DIVIDERS, WRITE CLOCK GEN., BIT COUNTER, TAPE SPEED SELECT 2

TAPE UNIT SELECT DECODE 6

TAPE UNIT CONTROL 7
MODE CONTROL
COMMAND REGISTER

WRITE CLOCK GENERATOR 8

PHASE ENCODERS 5

ODD PARITY GEN. 3

WRITE DATA STORAGE REGISTERS 3

2 TRACK MONITOR & TRACK SWITCH 17

"WINDOW" CLOCK GENERATOR (VFO) 14

REVERSE MODE INVERTERS 15 (9 CHANNELS)

BIT SYNC AND DECODERS 15 (9 CHANNELS)

4-STAGE DESKEW BUFFERS AND READ WRITE COUNTERS 15 (9 CHANNELS)

IBG, FILE MARK, I.D. DETECTORS 13

FM/ID (TO STATUS REGISTER)

TRACK DROPOUT DETECT AND "DEAD TRACK" REGISTERS 13

FROM READ CONTROL

BOV
B FULL

STATUS LOGIC AND REGISTER 5 6

SKEW ERROR DETECT (FROM READ CONTROL)
ERROR CORRECTION (CER)
FALSE PREAMBLE DETECT } FROM READ CONTROL
FALSE POSTAMBLE DETECT
IDENT. DETECT } FROM FM/ID DETECTORS
FILE MARK DETECT
MULTI-TRACK DROPOUT

TO DELAY COUNTER

WRITE CONTROL 8

WRITE CLOCK
COMMAND REGISTER

ERASE 3" GAP
AUTO WRITE IB BURST AT BOT 8
PREAMBLE GENERATE 8
POSTAMBLE GENERATE 8
FILE MARK GENERATE 8

IBG DETECTOR
FROM DELAY COUNTER CONTROL
FROM READ CONTROL
FROM WRITE CONTROL

STATE COUNTER AND CONTROL 1

TO T.U. CONTROL
WRITE CONTROL
READ CONTROL

COMMAND REGISTER 7

VLD

TO COMPUTER ADAPTER CONTROL & RESET LOGIC

FORMATTER ADDRESS SELECT 9

VALID/REJECT LOGIC 6

TO STATUS REGISTER

TO TAPE UNIT CONTROL

MODE CONTROL 5

DATA TRANSFER LOGIC 16

WRITE STORAGE STROBE

POST AMBLE DETECT

READ CLOCK ACTIVITY SENSE 9

BOV
B FULL
COMMAND REGISTER
IBG

READ CONTROL AND DATA GATE 16

TO STATE COUNTER

(FROM VALID/REJECT LOGIC)
VLD

COMPUTER ADAPTER INTERFACE CONTROL 9

FROM RBSA

POST AMBLE DETECTOR 11

ODD PARITY CHECK 12

FALSE PREAMBLE/POSTAMBLE
SKEW ERROR (TO STATUS REGISTER)

BUFFER TRANSFER CLOCK

READ BUFFER STORAGE REGISTERS 11

TO POST-AMBLE DETECTOR

ERROR CORRECTION LOGIC (9 CHANNELS) 15

(CER) TO STATUS REGISTER

STATE COUNTER
SPEED CLOCK
COMMAND REGISTER
TRANS. TYPE STATUS
FROM WRITE CONTROL

DELAY COUNTER AND CONTROL 4

TO STATE COUNTER CONTROL

POR

RESET LOGIC 7

POWER ON
EXT. RESET
VLD

Figure 3-1. 1600 PE Formatter Block Diagram

starting from beginning of tape (BOT). The correct timing delays for erasing the inter-record gap (IRG) are provided and the file mark format is developed by the Formatter. The preamble and postamble are generated by the Formatter when writing, and automatic data error correction is performed by the Formatter when reading if there should be a single-track drop-out. The preamble and postamble is stripped off when reading.

The task of writing is reduced to mere transfer of the characters on a demand-response basis for the computer adapter logic.

The Formatter also reduces the reading and spacing operations to a minimum by performing all parity checks and positioning of the head in the IRG's automatically. The task of reading is reduced to transfer of the characters on a demand-response basis.

The Formatter can accommodate as many as four magnetic tape transport units simultaneously. All input/output signal lines are "daisy chained" to the multiple tape transports, while a single select line is wired to each individual tape transport. Only the selected tape transport unit will respond to the Formatter commands.

3.2 BLOCK DIAGRAM

A simplified block diagram of the 1600 PE Formatter is shown in Figure 3-1. The block diagram illustrates the various functions performed by the 1600 PE Formatter and shows the relationship between the Formatter, the tape transport units, and the computer adapter.

The circled numbers refer to the number of the logic diagram on which the indicated function is drawn in detail. This number is located in the lower right hand corner of the detailed logic drawings. Logic 9 illustrates the computer adapter interface.

3.2.1 Command Register & Valid/Reject Logic

When the computer outputs a command, the computer adapter supplies the command, and a strobe pulse to the Formatter Valid-Command-Detect logic. If the command is acceptable, a Valid clock is generated to enable the command to be loaded into the command register. If the command is not Valid, a "Reject" pulse is returned to the computer adapter. Each Valid clock initiates a System Reset (SRS) pulse, which is, in turn, used to reset the Formatter to initial conditions.

3.2.2 Computer Adapter Interface Control

The Valid clock also sets the Controller-Busy flip-flop. The Controller-Busy flip-flop normally is used by the computer adapter to signal termination of all commands. The State Counter and Control logic resets the Controller-Busy flip-flop after all tape motion has ceased for the commanded function. If "on-the-fly" writing or reading is desired, the Data Busy signal termination must be used by the computer to check status, then initiate the next command.

3.2.3 Tape-Unit Control

The Tape-Unit Control logic develops the Forward, Reverse, Rewind and Offline commands to the selected tape transport unit under control of the command register and the Mode Control.

3.2.4 Formatter Select

The Formatter-Select logic allows a Formatter to be assigned the number "zero", or "one", so that two Formatters can be "Daisy-Chain"-connected to one computer adapter to control up to eight transports or a mixture of NRZI and 1600 CPI Phase Encoded Transports.

3.2.5 Tape Unit Select

The Tape-Unit-Select switches allow the operator to assign numbers 0, 1, 2 or 3 to any of the four tape units. This allows tape units to be switched without requiring changes to the computer program. Indicator lamps give visual indication of which tape unit is selected.

3.2.6 State Counter and Main Control

The State Counter breaks the major operations (such as Write and Read) into successive "sub-states" that are sequentially stepped through to perform the operation. These states are:

State Count	Function
0	Rest
1	Predelay (not BOT and not 3-inch gap)
2	Predelay (BOT or 3-inch gap)
3	Write or Read execution
4	Postdelay
5	Forward Motion Halt time out
6	Reverse Motion Halt time out
7	Rewind or Clear execution

The "delay" and "time out" states all use the Delay Counter to determine when the state count should terminate and the next state count be entered. These Delay-Count times vary, depending upon factors such as:

1. Tape speed
2. Single or dual-stack head
3. Edit or normal mode
4. Reverse or Forward motion

The pre- and post-delays are used to erase the Inter-Record Gaps (IRG) and to halt the head in the correct position in the IRG when reading.

State 0 (the "rest" state) is the state the Formatter enters after completing an operation.

In State 1 (Predelay) the Formatter waits for the tape unit to get up to speed and erases part of the IRG when writing. State 1 is used for predelay when not starting from BOT or not erasing a 3-inch gap.

State 2 (Predelay) is similar to State 1, except a longer delay accommodates the Erase-3-Inch-Gap Command as well as the automatic erasing of the 3-inch gap at BOT.

In State 3 (Write or Read Execution), the record is written or read. When reading, State 3 is terminated when no more read strobes occur, indicating that the IRG has been reached.

IRG detection is also used to terminate State 3 for write operations when using dual-stack, read-after-write tape unit (so that the written record can be checked for correct parity). For single-stack writes, State 3 is terminated as soon as the postamble is written at the end of the record.

State 4 (Postdelay) is used to halt the head in the correct position in the IRG when reading. When writing, State 4 postdelay erases a portion of the IRG.

State 5 (Forward Motion Halt Time Out) retains memory of the forward direction of motion during the time that elapses between the issuance of the Stop Command and the actual stopping of the machine. This delays termination of the CBUSY signal until the tape unit has completely halted in the IRG.

The DBUSY status terminates when State 5 is entered, so that successive "Writes" or successive "Reads" may be executed, "on-the-fly" without stopping in the IRG's.

State 6 (Reverse Motion Halt Time Out) is similar to State 5 except for reverse motion commands. When performing, "on-the-fly" operations, successive commands issued after DBUSY terminates, but before CBUSY terminates, must be of the same type. A Read cannot follow a Write and a Forward Motion command cannot follow a Reverse Motion command (or vice versa). There is, of course, no such restriction if the commands are not issued until after CBUSY terminates.

State 7 (Rewind or Clear) is entered upon issuance of a Rewind or Clear command by the computer. The State is terminated when the tape unit finishes rewinding.

3.2.7 Mode Control Logic

The Mode Control logic drives the Tape Unit Control to provide Threshold control and Edit mode as well as Multiple Record Spacing control.

3.2.8 Status Register

The Status Register stores both the tape unit status and the Formatter status so that the computer can inspect the results of an operation to find out whether the operation was completed correctly or some other action needs to be taken. The register is reset by the POR pulse when a valid command is initiated. The status of the selected tape unit and the Formatter are available for access by the computer at any time.

3.2.9 Read Activity Sense

The Read Activity Sense logic is used to signal activity of each record. The Check-Word-Count (CKWDCNT) pulse occurs when the Postamble is detected. The CKWDCNT pulse is delivered to the Computer Adapter interface, where it may be used to create an extra data transfer request to the computer for the case where an odd number of characters were read from tape and the "Pack" mode of operation is being used. The CKWDCNT pulse is also typically used by the Computer Adapter to determine if the expected number of characters were read from tape. It creates status bits to inform the computer that the record was too long, too short and/or contained an odd number of tape characters.

3.2.10 IBG, File Mark, Phase Mode Identification Burst Detectors

The File-Mark-Detect logic checks for the file mark from the dead track logic. The EOF status bit is developed if a file mark is detected in a forward or a backward direction. The Interblock Gap Detector terminates the Read control logic if the Halt signal from the Data Transfer logic is missing at the end of a record. The IBG signal is also used to advance the State Counter to the Postdelay state. The PE ID detector sets the IDENTS status bit if the ID burst is detected at BOT.

3.2.11 Read Control Logic

The Read Control Logic controls data transfer during State 3 until the IBG is detected, at which time the Postdelay (State 4) or one of the Halt delays (State 5 or 6) is entered.

When the IBG is detected or the computer generates the Halt signal (to indicate it doesn't want any more data), there are no more Data Flag signals generated even though there may be more data in the record.

The Read Control Logic also controls the Forward and Reverse Space operations. These operations are identical to reading forward or reverse except the Data Flag is not set for data transfer requests. All parity checks are valid for the spacing operations as well as the reading operations and for read-after-write operations, when a dual-stack head is employed on the selected tape unit.

Special read modes may also be used:

1. Read threshold high
2. Read threshold extra low

The Read Threshold High mode may be used with a single-stack read/write tape-unit to enable a marginal parity check to be performed on each record immediately after it is written. This is accomplished by back-spacing over the record and spacing or reading forward over the record in the Read Threshold High mode, then checking for parity error status. This marginal-check function is automatically performed by dual-stack read-after-write tape units, since they automatically select the high threshold when in the write mode so that the read-after-write parity checks may be performed while writing.

The Read Threshold Extra Low mode allows tape units equipped with this option to recover low amplitude signals on poor quality tapes.

3.2.12 Two-Track Monitor and Track Switch

This logic takes bit transitions from a single "Master" track to control the Phase-lock-loop oscillator, which generates the 16-times-the-bit-rate "Window Clock".

If the selected track should have a drop-out, the logic will switch to the alternate track. Tracks 2 and 6 are used.

3.2.13 Window Clock Generator

The Window Clock Generator is a phase-locked-loop variable-frequency oscillator capable of tracking data-rate variations of up to ±10% of nominal. The Window Clock is 16 times the bit-rate to allow the Bit Sync and Decoder logic to divide each bit-period into 16 periods. Thus, a "window" can be generated ±25% around the nominal bit-transition time. This allows the optimum window to be generated to mask out any "phase" transitions in the middle of the bit period.

3.2.14 Reverse-Mode Inverters

The reverse-mode inverters invert the data signals in the Reverse operations so that the postamble can be interpreted as a preamble in the reverse direction. There is one circuit per track, for a total of 9 circuits.

3.2.15 Bit Sync and Decoders

These consist of nine circuits (one per track) and they synchronize to the bit-transitions (ignoring phase transitions) and decode the data signals to develop logic levels for ones and zeroes. The Bit-Sync logic synchronizes on the 40 zeroes in the preamble, using a "window counter" per track. It then operates on the bit-transitions throughout the record, while masking out the phase transitions with the window counters.

The decoders also signal the dead track detectors if the 25% maximum limit of the window is reached.

3.2.16 De-Skew Buffers and Read-In Counters (RIC)

The De-Skew Buffers and RIC's are duplicated for each track and provide four bits of deskewing. The RIC's keep track of each bit placement in the deskew buffers and control the Buffer-Full (BFULL) signal to indicate when a new character has been deskewed and assembled.

The RIC's begin operating after the "all-ones" pattern at the end of the preamble has been detected, hence they "strip off" the preamble.

The RIC's also indicate a skew error (if there are more than four bits of skew between any two tracks) by generating the buffer overflow (BOV) signal. The outputs of the four-bit deskew buffers are multiplexed to a single line per track by the RIC's. Each track accomplishes the deskewing by always offering the oldest bit in each buffer to the Error Correction logic.

The "Dead Track" register controls the RIC multiplexer such that the RIC is disabled from the Preamble Detection, Postamble Detection, Buffer Full and Buffer Overflow logic. Therefore, the Formatter can continue operation normally (and correct data) if only a single track is "dead".

3.2.17 Postamble Detector

The Postamble Detector detects the occurrence of an "all-ones" pattern in the first stage of the Dual-Read Storage Registers and the next character (on the multiplexed output bus of the deskew buffers) containing all zeroes. The Postamble Detection logic disables the Buffer Transfer clock and the Data Flag signal to "strip off" the postamble.

3.2.18 Odd Parity Check

The Parity Check logic monitors the RIC-multiplexed bus from the deskew buffers and provides the error signal to the Correction logic so that, for a single dead track and a parity error, the data for the affected track can be inverted to provide correction.

The Corrected Error (CER) signal is supplied to the Status Register for this condition.

3.2.19 Error Correction Logic

The Error Correction logic inverts the data in the dead track when a parity error and a single track is dead.

3.2.20 Track Drop-Out Detect and Dead Track Register

This logic is duplicated for each track and operates with the "window" counters such that a bit is said to have been "dropped" if the Window Counter reaches 25% greater than the nominal bit period.

The Dead Track register stores this information for status and to develop the "Single Dead Track" and "Multiple Dead Track" signals.

3.2.21 Read Buffer Storage Registers

The Read Buffer storage consists of two stages of character storage to allow the postamble to be "stripped" from the data. Two stages are needed because the postamble detection doesn't operate until the second character (the all-zeroes following the all-ones character) is detected. Hence, the decision on whether to set the data flag must be delayed by an extra character time.

3.2.22 Write Storage-Registers

The Write Storage-Registers are provided so that no register is needed on the Computer Adapter to store output data from the computer. The Data Transfer logic operates on a request/response basis via the Data Flag and Write/Read Acknowledge (W/R ACK) signals such that each character is requested a full write-clock period before it is needed and the computer can respond any time within this period with a W/R ACK strobe pulse to load the Write Data into the first stage of the Write Storage Registers. The

second stage is then loaded from the first stage at the bit time. The Phase Encoders then utilize the second-stage bits to control inversion or non-inversion of the clock frequency square wave to encode the data into the phase encoded format.

3.2.23 Parity Generator

The Parity Generator creates odd parity for each character presented from the first stage of the Write Storage Register and sends the parity bit to the second stage.

3.2.24 Phase Encoders

The Phase Encoders convert the logic levels from the second stage of the Write Storage Register to phase encoded format by inverting the square wave clock signal for logic "ones" and passing the clock for logic "zeroes".

3.2.25 File Mark Generator

The File Mark Generator generates the file mark format (40 "zero" bits) in tracks 0, 2, 5, 6, 7, P with tracks 1, 3, and 4 erased. This is the IBM format file mark, but is compatible with the ANSI specifications which are: 32 to 128 zeroes in tracks 2, 6 and 7 with anything in tracks 0, 5 and P while tracks 1, 2 and 4 are erased.

3.2.26 Preamble Generator

The Preamble Generator inserts 40 zeroes followed by an "all-ones" character before each data record.

3.2.27 Postamble Generator

The Postamble Generator inserts an "all-ones" character followed by 40 zeroes after each data record.

3.2.28 Auto Write ID Burst at BOT

This logic writes alternating "ones" and "zeroes" in the parity track while erasing all other tracks in the BOT tab area when initiating a write or write file mark from BOT.

3.2.29 Erase 3" Gap

This logic causes a 3-inch section of tape to be erased.

3.2.30 Write Control Logic

The Write Control Logic operates during State 3 for Write, Erase, and Write File Mark operations. The Write Control Logic controls the preamble generation then controls the Data Transfer Logic for write operations by developing the Set Data Flag pulse to request each character to be written until the Write operation is terminated by the Halt signal from the Computer Adapter.

Upon receiving the Halt signal, the postamble is automatically appended to the record and part of the IRG is then erased. If a single stack (read/write) tape unit is selected, the Write Control Logic triggers the State Counter to the State 4 postdelay when it finishes writing the postamble at the end of the record. If a dual-stack (read-after-write) tape unit is selected, the Inter-Record Gap Detect logic is used to exit State 3 to State 4 Post Delay in order to allow all of the record to be Read-After-Write parity-checked.

3.2.31 Write Clock Generator

The Write Clock is developed from the Crystal Oscillators and Tape-Speed Select logic. The clock is at twice the bit-rate and operates for the ID burst, the Write File Mark and the Write One Record operations.

3.2.32 Crystal Oscillator and Tape-Speed Select

The Crystal Oscillator provides a stable, precision clock frequency for 1600 bits-per-inch packing density. The Tape-Speed Select logic divides down the crystal oscillator to the appropriate frequency and selects the Write clock frequency dependent upon tape speed and packing density. One crystal covers the standard tape speeds from 12.5 to 112.5 ips.

The Speed Clock signal is used by the Delay Counter to provide all the precise time delays for the Formatter. The Bit Counter provides a count of bits to control the 41-bit-length preamble and postamble as well as the 40-bit-length file mark.

3.2.33 Data Transfer Control

The Data Transfer Control operates in conjunction with the Read or Write Control logic depending upon whether a Read or Write operation is active.

The Read or Write Control logic generates the Set Data Flag pulse to signal that Read data is ready for input or to request a Write Data character. The Computer Adapter returns the W/R ACK signal, which clears the Data Flag and is used to strobe the Write data into the Write Storage Register for write operations. When the Computer Adapter desires to halt data transfer, it generates the HALT signal and the Data Flag signal is disabled.

The WRMSB signal is generated to allow the computer adapter to "unpack" a computer word into two tape characters.

3.2.34 Delay Counter

The Delay Counter is a flip-flop divider-chain that counts the Speed Clock pulses to provide precise time intervals for Pre- and Post-delays as well as Halt delays. The time interval is defined by the interval between the time the counter is allowed to start counting (from a reset condition) and the time that the STOP signal is generated by a set of gates that decode various counts from the Delay Counter. The gate selected for a particular time interval is dependent on which state the Formatter is in as well as on the configuration of the Formatter and the selected tape unit (provided by the STATUS signals to the Delay Counter).

3.2.35 Reset Logic

The Reset Logic generates a System Reset (POR) pulse when a valid command is initiated. This resets the Formatter to initial conditions and clears the status register. The POR pulse is also generated to clear the Formatter when the power is turned on or when the computer adapter generates an External Reset pulse.

3.3 FORMATTER COMMANDS

3.3.1 Basic Commands

Basic Commands provided by the Formatter are:

1. Read (one record)
2. Write (one record)
3. Space
4. Write File Mark
5. Erase 3-inch gap
6. Rewind
7. Offline
8. Clear

3.3.1.1 Read and Space

The Read and Space operations can be in the forward or reverse direction in one of three possible modes (Normal, Read Threshold High or Read Threshold Low). In addition, a Read Forward may be performed in a "Test Read" mode in which the CRC and LRC characters are input to allow diagnostic programs to check the CRC and LRC generator circuits. The Read Threshold High mode is used with single-stack-head (read/write) tape-units to allow marginal checking of each record immediately after it is written. This is accomplished by backspacing over the record and reading, or spacing forward in the Read Threshold High mode and checking for no parity errors. The Read Threshold Low mode provides the ability to recover low amplitude data from poor quality tapes (if the tape unit is equipped with this option.

The space operations can be a single or multiple record under control of the STOP SPACE Computer Adapter signal. In addition, the back-space operation can be conducted in the EDIT mode to position the write head correctly in the IRG preceeding a record that is to be replaced with an equal length but updated record. BOT will halt backspacing automatically.

3.3.1.2 Write, Erase 3-Inch Gap and Write File Mark

The Erase 3-Inch Gap command can be performed by itself or combined with the Write or Write File Mark commands to cause a three-inch gap to be erased prior to writing the record or file mark. A Write command can be performed in the EDIT mode (if the record to be replaced has first been backspaced over in the EDIT mode to position the head correctly) to replace one record with an updated record of equal length.

3.3.1.3 Rewind and Offline

The Rewind command causes the selected tape unit to rewind to Load Point (Beginning of Tape). The Formatter can optionally go "Busy" until the rewind is terminated (to provide a means of interrupting the computer upon termination of the operation) or not.

The Offline command never sets the Formatter to the "Busy" state and may be sent to a selected tape unit even if the tape unit is "Not Ready" because it is performing a rewind operation.

3.3.1.4 Clear

The Clear command can be used to clear the status register and set the Formatter to initial conditions, even if the Formatter is "Busy". After the Clear command is generated, the Formatter will return to the "Not Busy" status.

3.3.2 Command and Mode Combinations

The commands executable by the Formatter depend on the "mode" lines and are listed in Table 3-1.

The Command signals are strobed into a command storage register in the Formatter by the Command Clock (STROBEC), hence can be changed immediately after the termination of the STROBEC pulse. The MODE lines must be held static throughout each operation, since no storage is provided in the Formatter.

Table 3-1. Command and Mode Combinations

FORMATTER OPERATION	"SET XXX" COMMAND SIGNALS									"MODE" SIGNALS				
	REV	WCC	WFM	GAP	FSR	RCC	CLR	REW	OFL	THR1	THR2	EDIT	TRD	STOP SPACE
1. Test Read Forward						X				1	2		X	
2. Read Forward						X				1	2			
3. Read Reverse	X					X				1	2			
4. Write 1 Record (normal)		X												
5. Write 1 Record (Edit)		X										X		
6. Space Forward 1 record					X					1	2			
7. Space Forward "n" records					X					1	2			3
8. Space Reverse 1 record	X									1	2			
9. Space Reverse "n" records	X									1	2			3
10. Space Reverse (Edit mode)	X									1	2	X		
11. Write File Mark			X									4		
12. Erase 3 Inch Gap				X										
13. Erase 3" then Write File Mark			X	X										
14. Erase 3" then Write 1 record		X		X										
15. Rewind								X						
16. Offline									X					
17. Initiate Rewind then Offline								X	X					
18. Clear							X							

SEE NEXT PAGE FOR NOTES 1 - 4.

NOTE 1 The THR1 mode (Read Threshold High) has no effect except when reading with single-stack-head (read/write) tape units equipped with this feature. THR1 allows for a marginal checking of written records by back-spacing, then marginal checking during a Read or Space Forward operation.

NOTE 2 The THR2 mode (Read Threshold Low) has no effect unless the selected tape unit is equipped with this feature. THR2 allows recovery of low-amplitude data from poor quality tapes.

NOTE 3 The STOP SPACE signal is used only for continuous spacing over multiple records. The DBY signal can be used by the Computer Adapter to count records to determine when the required number of records has been traversed.

NOTE 4 The Edit mode can be used to rewrite a file mark if the file mark is first backspaced over in the Edit mode.

3.4 STATE FLOW

Figure 3-2 illustrates, in simplified form, the State Counts through which the Formatter sequences. Figure 3-3 illustrates the State Flow in detail.

3.4.1 Simplified State Flow (See Figure 3-2)

The Formatter is in the "Rest" State 0 at initial conditions. The Strobe C command clock is rejected if the command is not a "valid" one. If CBUSY is not set by a valid command, then the command must be:

1. Offline
2. Rewind (with no interrupt)

In this event, the command is executed, but the Formatter remains in State 0.

If CBUSY is set, then a Rewind or Clear command causes the Formatter to enter State 7 until the rewinding status signal is false. At this time CBUSY is cleared and State 0 is re-entered. For a Clear command (since the rewind status bit never is true), CBUSY is cleared almost immediately.

Any other command causes one of the two Predelay states to be entered. State 1 is normally used, but State 2 is used when the Formatter is at BOT or a 3-inch Gap Command is executed. The appropriate motion signal (SFC for forward motion, SRC for reverse motion) is activated at this time.

The predelays are used to erase a 3-inch gap or part of the IRG when writing and to allow sufficient time for the tape unit to get up to speed.

The State 3 data transfer then takes place. For writing, the data is written until the HALT signal from the Computer Adapter terminates the record. For "Erase", no data transfer is needed, so State 3 is terminated immediately and State 4 is entered. For "Write File Mark" no data transfer actually occurs, but the Formatter writes the file mark and the LRC character and then enters State 4.

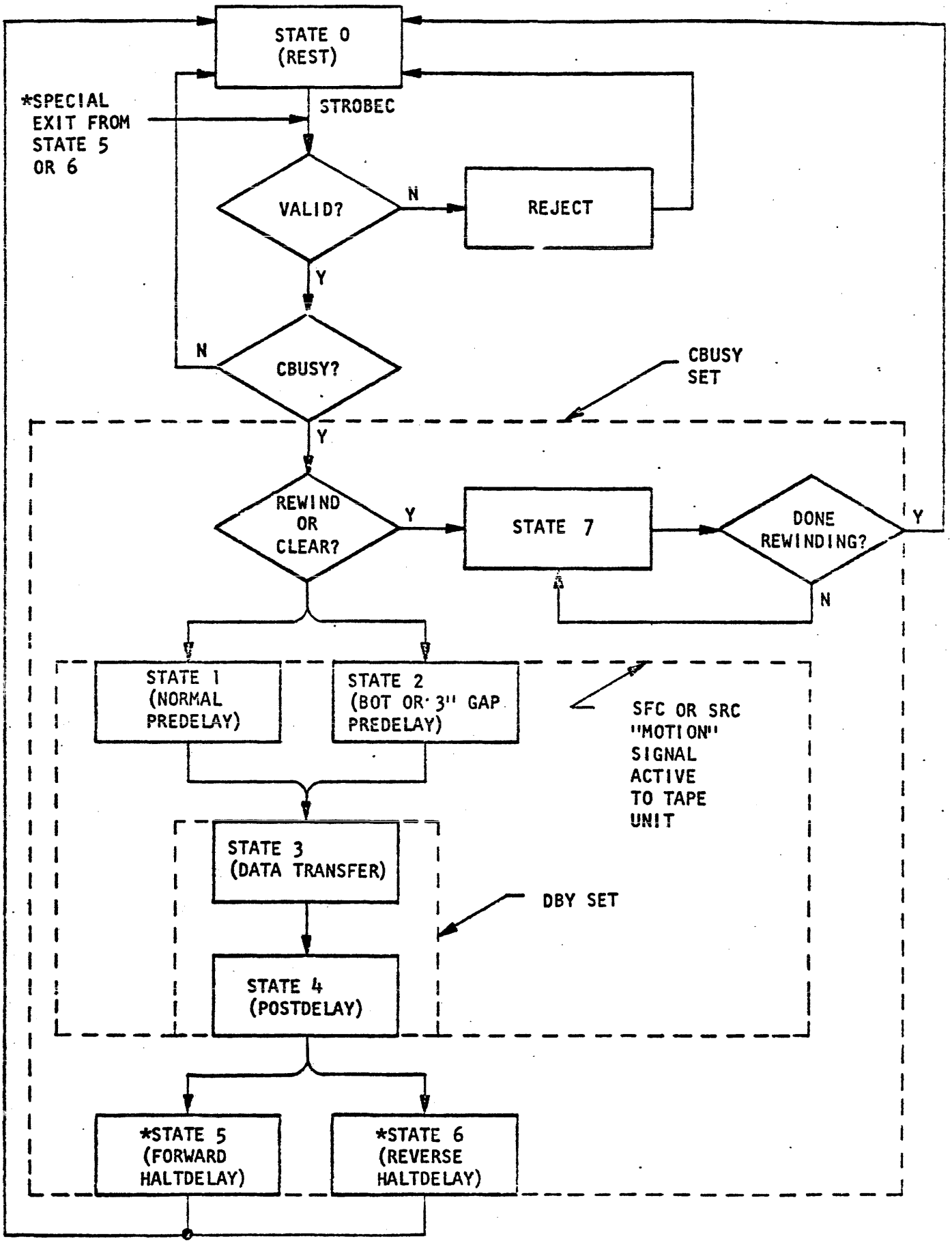


Figure 3-2. Simplified State Flow

For dual-gap (read-after-write) tape units, the transition from State 3 to State 4 is delayed until the read-head detects the end of the record (the beginning of the IRG). This allows the full record to be checked for parity errors. State 4 Postdelay (in conjunction with the .2-inch distance the tape moves after the motion command terminates) is used to erase the first part of the IRG.

For Reading or Spacing operation, State 3 is maintained until the end of the record and the IRG is reached. For reading, the Computer Adapter HALT signal terminates actual data exchange. For reading or spacing, the State 4 Postdelay (in conjunction with the fixed .2-inch distance the tape moves when halting after the motion command terminates) is used to position the head in the correct position in the IRG to allow for a subsequent Write or Read operation.

Note that the Data Busy (DBY) signal is active only during States 3 and 4, while the "motion" signals to the tape unit are active from the beginning of the Predelay State through the Postdelay State.

After the Postdelay occurs, one of the forward/reverse Halt Delay (State 5 or 6) is entered to insure that the tape is allowed sufficient time to come to a halt in the IRG.

At the termination of the Halt Delay signal, CBUSY is cleared (to signal the computer that the next command can now be executed) and the Rest State 0 is entered.

The "Special Exit" from State 5 or 6 allows continuous writing or reading without stopping in the inter-record gap to optimize data transfer efficiency.

Since the Start/Stop characteristics of the tape units are ramp-like, the gap-traverse time is twice as long (as it would be at full speed) when the next command is delayed until the tape has completely halted.

This "Special Exit" allows a write or read command to terminate the Halt Delay State and initiate the Predelay State without getting "rejected" even though the CBUSY signal is active.

In any other State, with CBUSY active, a command (other than clear) is rejected.

The computer can accomplish "on-the-fly" writing or reading by initiating the next command when DBY terminates at the end of State 4, rather than waiting until DBUSY terminates. However, there are certain restrictions on this type of operation:

1. The next command must not switch from a Write or Write File Mark to a Space or Read (or vice versa).
2. The next command must not be a Rewind or Offline if the previous command was a Write, or Write File Mark type.

It is the computer program's responsibility to make sure these restrictions are followed.

The Delay Counter is used in States 1, 2, 4, 5 and 6 to generate the prescribed delay times.

3.4.2 Detailed State Flow (See Figure 3-3)

The Detailed State Flow chart shows the control over signals DBY, CBUSY and the motion commands SFC and SRC, as well as the use of the Delay Counter. In all other respects, the flow chart is similar to Figure 3-2.

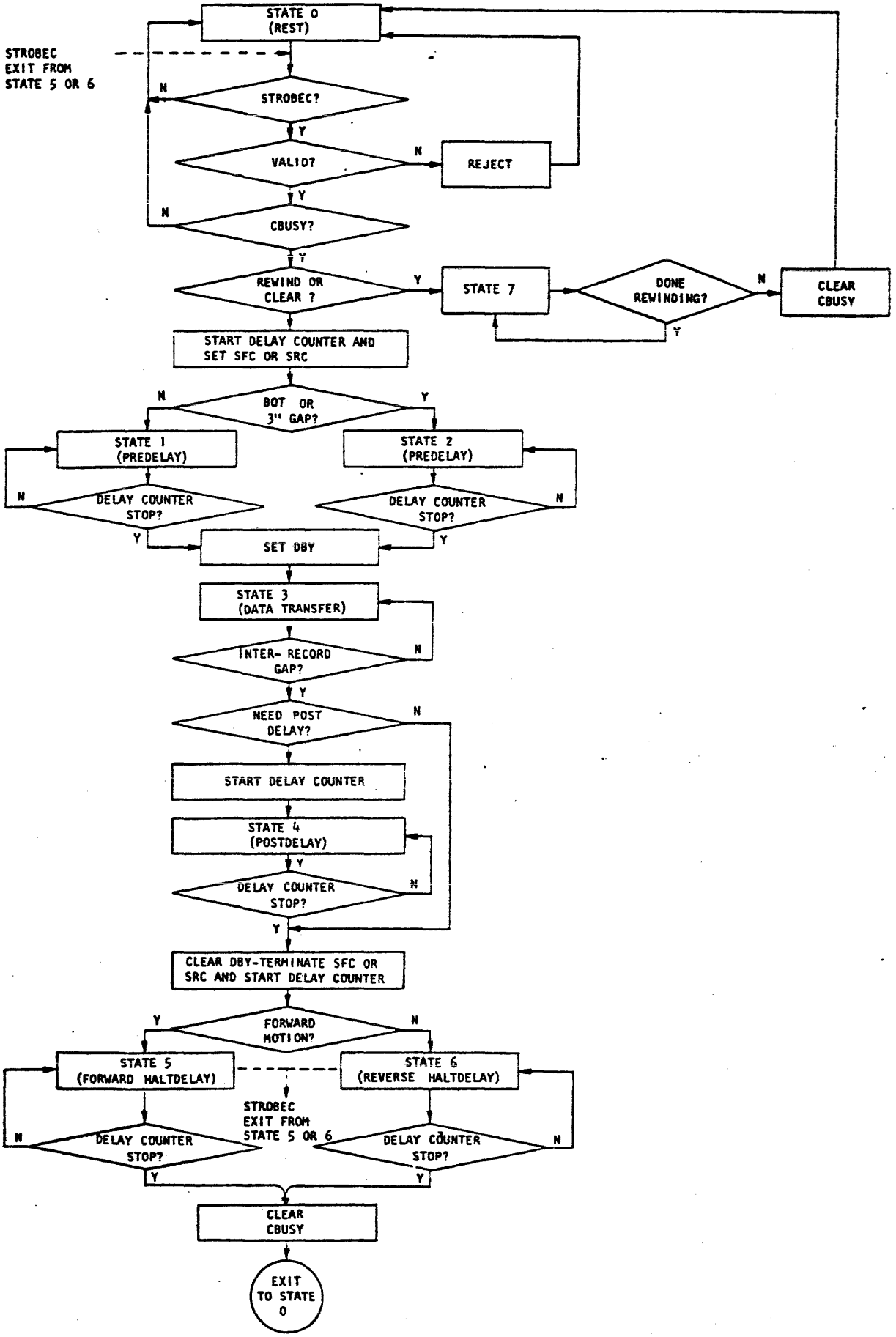


Figure 3-3. Detailed State Flow

In addition, the IRG detection exit from State 3 is detailed as is the detour around State 4 Postdelay (to achieve minimum Postdelay in certain cases.

3.5 COMMAND EXECUTION AND TIMING

The main commands are discussed step-by-step and an illustrative timing Diagram is included for each command.

The main commands are:

1. Clear
2. Rewind (with interrupt)
3. Write File Mark (7 track)
4. Write File Mark (9 track)
5. Forward Space 1 Record
6. Back Space 1 Record
7. Write 1 Record (7 track)
8. Write 1 Record (9 track)
9. Read 1 Record (7 track)
10. Read 1 Record (9 track)
11. Erase 3-inch Gap

3.5.1 Clear

The Clear function will terminate any motion command and reset the Formatter to initial conditions. CBUSY will set and then reset after the Clear command is complete to signify that the Formatter is ready for the next command.

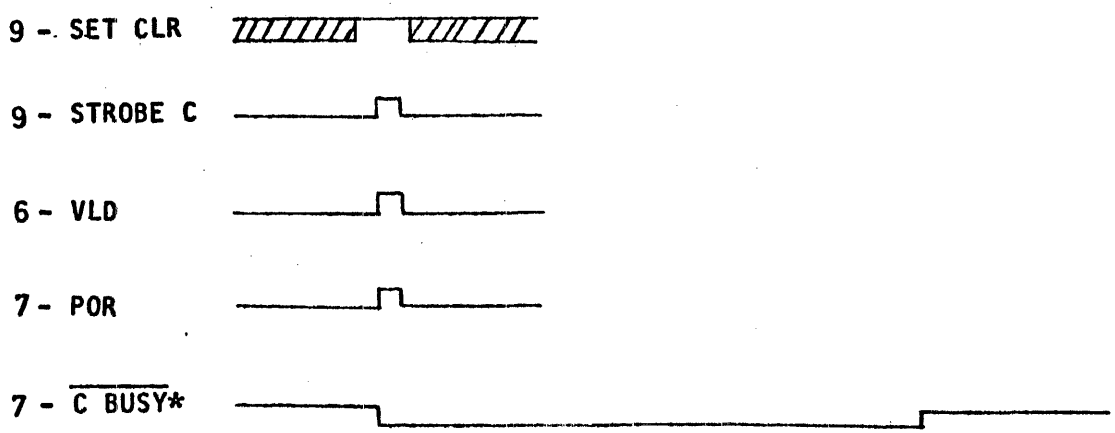


Figure 3.4. "Clear" Timing Diagram

The Clear command is included mainly to allow diagnostic programs control over a faulty Formatter that doesn't halt the tape unit. This command must not be used to halt any Write or Read operation, since the head will not be halted at the correct point in the IRG and the CRC/LRC characters won't be written or read.

The System Reset 7-POR* pulse resets the Status register.

3.5.2 Rewind (With Interrupt)

The offline command doesn't set CBUSY and neither does the Rewind command if the Rewind interrupt (see option 3.3.7) is jumpered out. In this event, the commands are passed on to the selected tape unit as a pulse.

If the rewind interrupt is not jumpered, CBUSY is set for a rewind command and resets when the rewind command is completed to signal the computer that the next command can be accepted by the tape unit.

Figure 3.5 illustrates the timing.

When the computer adapter generates the 9-STROBEC pulse while 9-SETREW is high and the Formatter isn't busy, the command is accepted and the 6-VLD pulse is generated.

The 7-REW flip-flop is set to store the rewind command. When the 9-STROBEC clock pulse terminates, the rewind command is generated to the selected tape unit (signal 7-$\overline{\text{RWC}}$). When the tape unit responds that it is rewinding (signal 10-REWINDING), the 7-REW flip-flop is reset and the Formatter 10-$\overline{\text{RWDG}}$ status bit is set. The tape unit goes "not ready" 10-$\overline{\text{RDY}}$) during a rewind. Since the tape-unit rewind terminates before the tape unit returns to load point and becomes "Ready" again, the 6-$\overline{\text{RWDG}}$ status bit is interlocked to wait until the tape unit goes ready 10-$\overline{\text{RDY}}$).

The 7-POR* (System Reset) pulse clears the status register.

At this time 7-$\overline{\text{CBUSY}}$* resets to signal that the operation is complete.

3.5.3 Write File Mark

When signal 9-SET WFM is high during the 9-STROBEC clock pulse, the 7-WFM command register flip-flop is set to initiate a Write-File-Mark command. The 7-POR* pulse is also generated to reset the Formatter to initial conditions. The 7-CBUSY flip-flop is set by the 6-VLD clock, and the 7-SFC command is activated to start the tape moving in the forward direction. Command register flip-flop 7-WFM also sets the selected tape transport unit to the write mode via signal 7-$\overline{\text{SWS}}$.

The Predelay signal delays writing of the file mark until the tape transport unit is up-to-speed and has generated a portion of the required inter-record gap. If the tape transport unit is at the beginning of tape (BOT) when the Write-File-Mark instruction is generated, the Predelay is longer to cause a 3-inch gap to be erased before the file mark is written. The Submode One (8-SM1) flip-flop is set upon the termination of the Predelay signal. The Gate-Write data strobe flip-flop (8-GWDS) is set to generate 80 write-strobes at twice the bit rate. Forty "zero" characters are written in tracks P, 0, 2, 5, 6, 7, while tracks 1, 3 and 4 are erased. Flip-flop 8-SM1 then resets and the Postdelay sequence is entered.

For a single-gap tape unit, the Postdelay is entered upon completion of writing the file mark. For a dual-gap tape unit, the delay counter is controlled by the interblock gap pulses to initiate the Postdelay after the file mark has passed the read head.

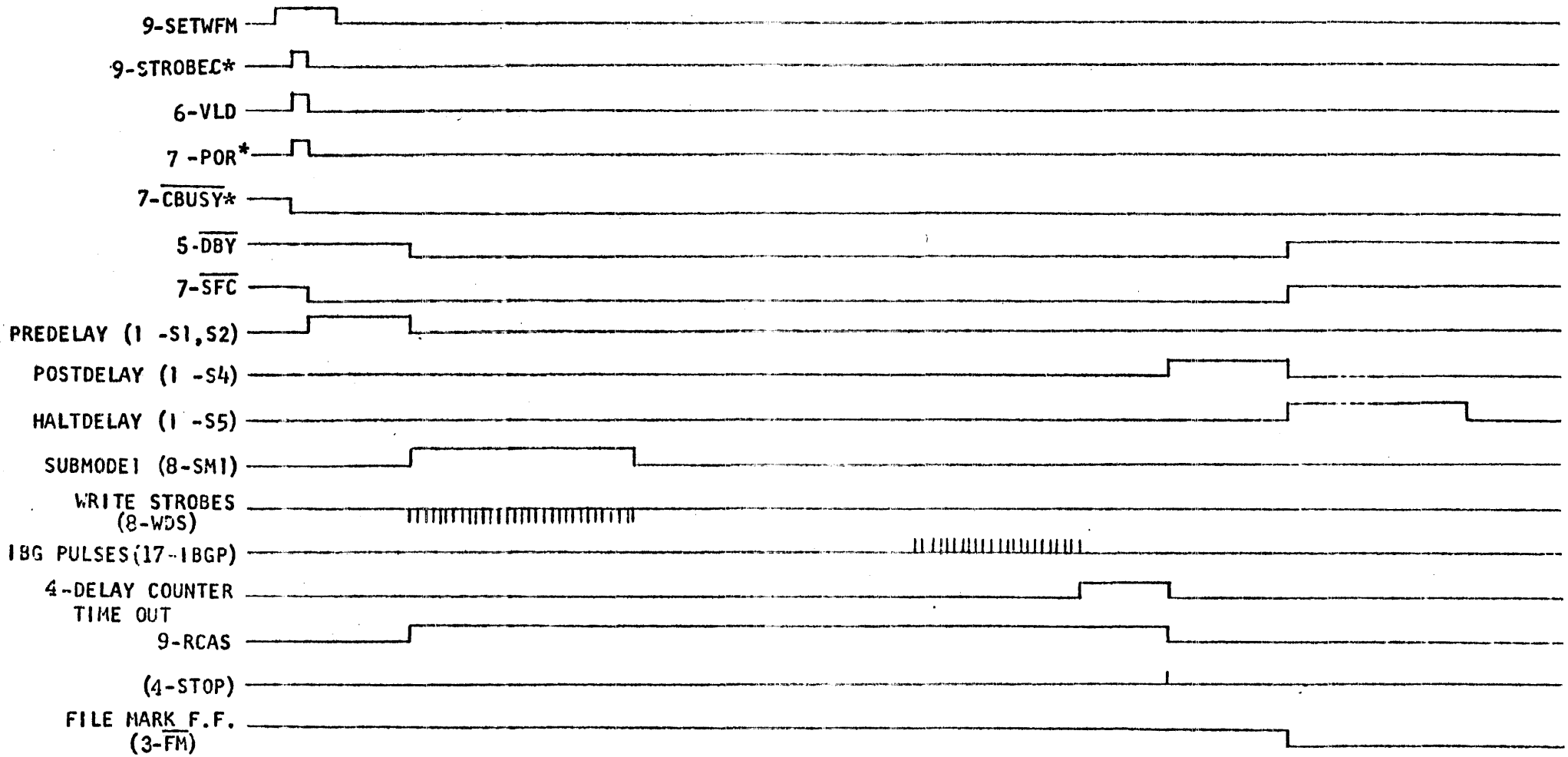


Figure 3.6. Write File Mark Timing Diagram

The Delay Counter is reset by each IBG pulse, and then times out a delay interval after the last pulse. Thus, the Delay Counter performs the task of IRG detection. Upon termination of the Delay Counter time out, the 4-STOP pulse is generated. The 4-STOP pulse is also used to trigger the State 4 Post-Delay circuits (1 -S4). When the Post-Delay terminates, the 7-$\overline{\text{SFC}}$ signal is terminated, and the State 5 Halt-Delay is entered. The Halt-Delay guarantees that the tape transport unit has ceased all motion in the inter-record gap. If the next command is to be a Write-type command, then the IRG can be erased at full tape-speed (without stopping in the IRG) by issuing the command after the signal 5-$\overline{\text{DBY}}$ terminates, rather than waiting until 7-$\overline{\text{CBUSY}}$ terminates. Status is valid after the 5-DBY signal terminates, hence the status can be checked before issuance of the next command.

3.5.4 Forward Space One Record

When term 9-SET FSR is high with the 9-STROBEC, the 7-$\overline{\text{SFC}}$ signal is activated to move tape forward. The 6-VLD and 7-POR* pulses are generated to reset the Formatter and initiate the space-forward operation.

NOTE The Space Forward command results in spacing over ONE record if signal 9-STOP SPACE is "open circuit" or at the High level. If multiple records are to be spaced over, 9-STOP SPACE must be held low until the leading edge of signal 9-$\overline{\text{RCAS}}$ occurs for the last record. The signal 9-$\overline{\text{RCAS}}$ may be used to count records to determine when the last record to be spaced over is reached, but the leading edge should be used to provide control over signal STOP SPACE. The 3-$\overline{\text{FM}}$ status signal and 6-$\overline{\text{EOTS}}$ status signal may also be used to switch STOP SPACE "high" so that a file mark or the end-of-tape will halt the multiple-record-spacing operation.

Note that 7-$\overline{\text{CBUSY}}$ remains low (for multiple spacing operations) until the final record has been passed.

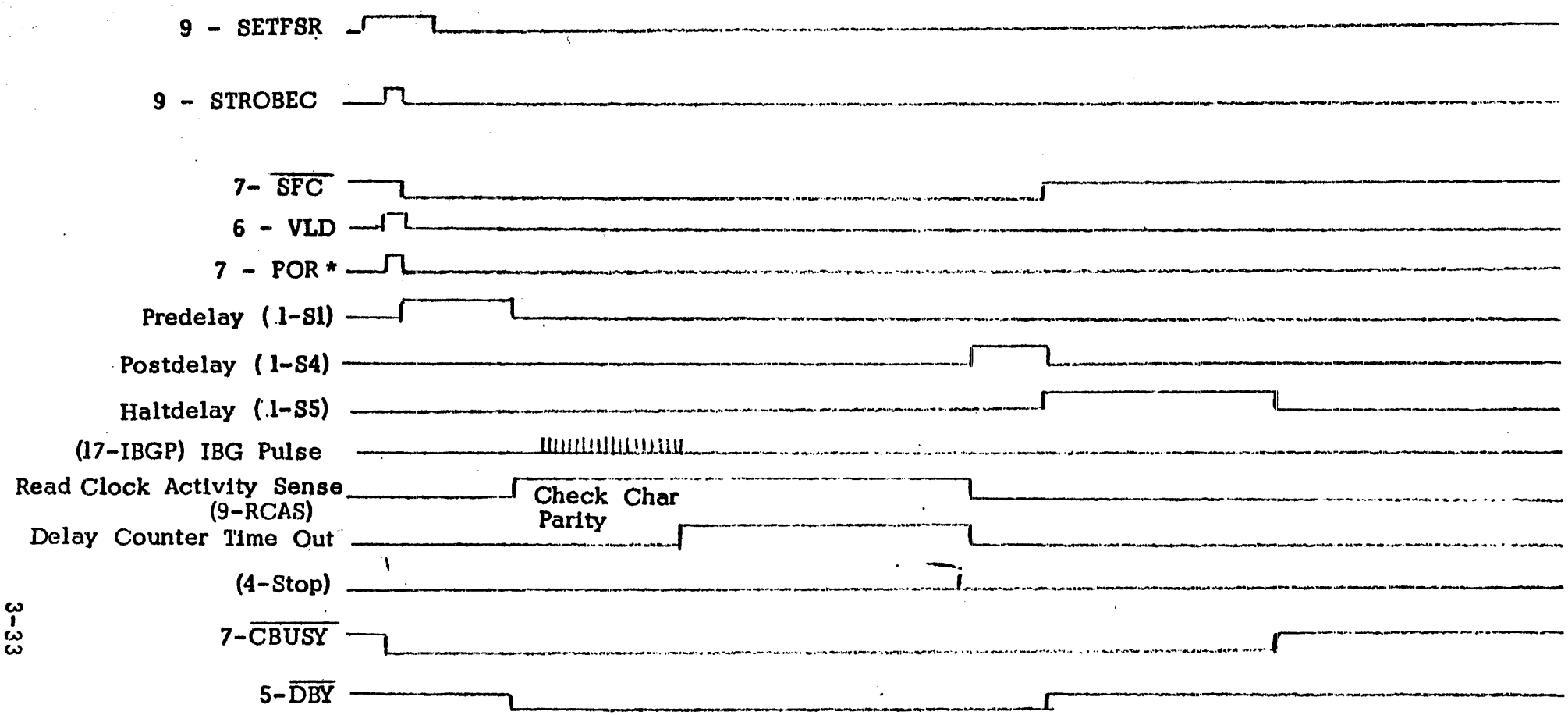


Figure 3.7 Forward Space One Record Timing Diagram

The Predelay allows the tape unit to get up to speed before allowing Read data to be accepted. The Read Clock Activity Sensor (9-RCAS) enables parity checks to be made while spacing. When the record is past, the Delay Counter times out to detect the IRG. After the Signal 5-$\overline{\text{DBY}}$ terminates, status can be checked and the next command can be issued (if a Read or Space Forward) to accomplish non-stop operation.

If no new command is issued at this time, the normal Halt Delay sequence is entered.

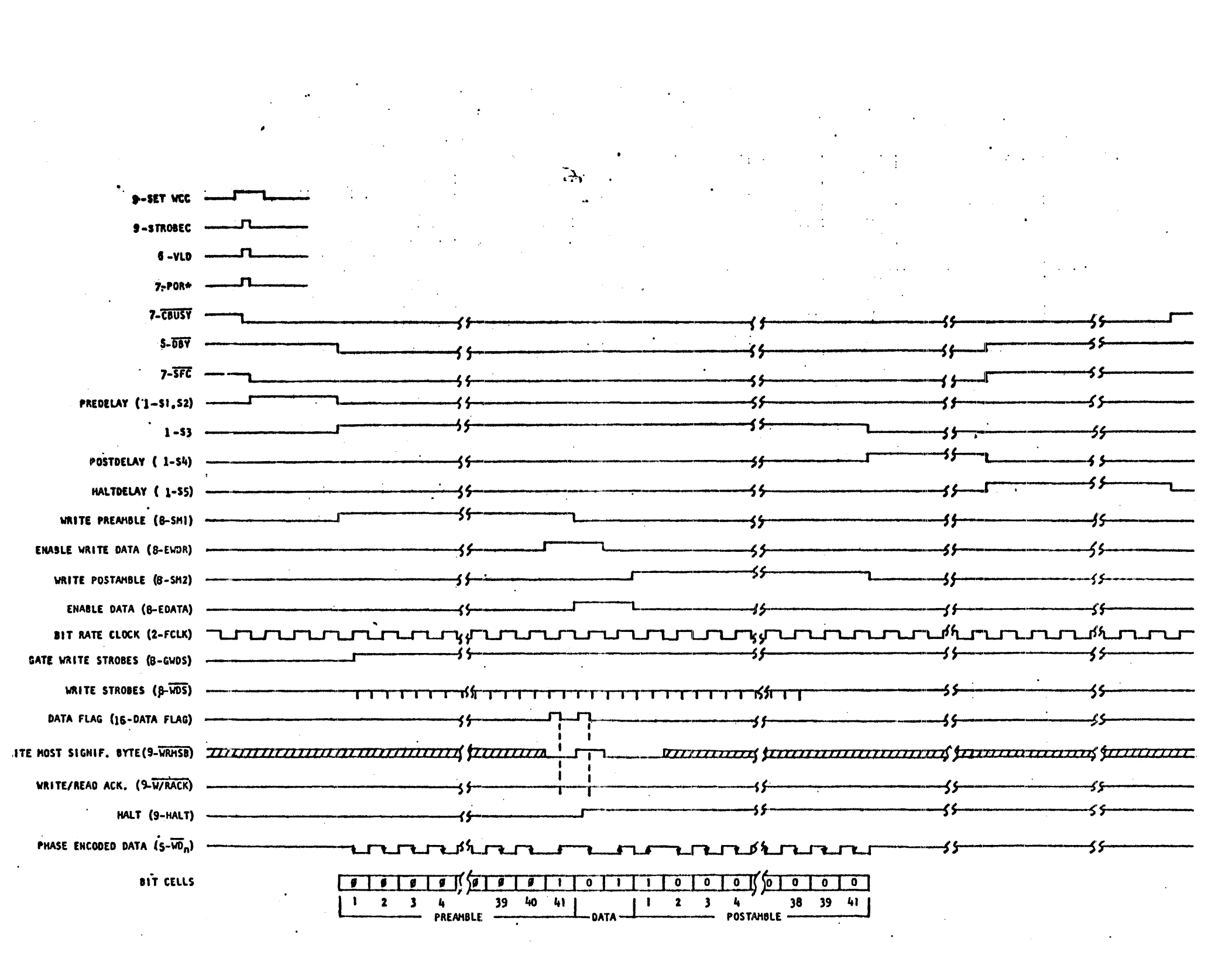
3.5.5 Backspace One Record

Backspace is similar to Forward space.

3.5.6 Write-One-Record (See Timing Diagram 3.8)

The write-one-record instruction causes the Formatter and the tape transport unit to turn-on the write current, enable the write amplifiers, get up to speed, generate a portion of the inter-record gap and write the preamble. Then the Formatter requests output data transfers from the computer adapter. The requested data-characters are written on tape until a HALT signal is generated by the computer adapter logic. The HALT signal causes the Formatter to terminate the record by writing the postamble.

The tape-transport unit Read-After-Write head enables parity checks to be performed upon the record that has just been written. After the parity checks are completed, the tape-transport unit erases a portion of the next inter-record gap and is then commanded to halt. After sufficient time has elapsed to ensure that the tape has completely stopped moving, then completion of the Write-One-Record operation is signaled when 7=$\overline{\text{CBUSY}}$ terminates.


9-SET WCC
9-STROBEC
6-VLD
7-POR*
7-$\overline{CBUSY}$
5-$\overline{DBV}$
7-$\overline{SFC}$
PREDELAY (1-S1,S2)
1-S3
POSTDELAY (1-S4)
HALTDELAY (1-S5)
WRITE PREAMBLE (8-SM1)
ENABLE WRITE DATA (8-EWDR)
WRITE POSTAMBLE (8-SM2)
ENABLE DATA (8-EDATA)
BIT RATE CLOCK (2-FCLK)
GATE WRITE STROBES (8-GWDS)
WRITE STROBES (8-$\overline{WDS}$)
DATA FLAG (16-DATA FLAG)
ITE MOST SIGNIF. BYTE(9-$\overline{WRMSB}$)
WRITE/READ ACK. (9-$\overline{W/RACK}$)
HALT (9-HALT)
PHASE ENCODED DATA (5-$\overline{WD_n}$)
BIT CELLS
0 0 0 0 0 0 0 1 0 1 1 0 0 0 0 0 0 0 0
1 2 3 4 39 40 41 1 2 3 4 38 39 41
PREAMBLE
DATA
POSTAMBLE

"On-the fly" generation of the IRG without stopping may be accomplished by checking status at the termination of signal 5-$\overline{\text{DBY}}$ and issuing the next Write, Erase or Write File Mark command immediately. The Write mode is set by the command clock (6-VLD) to initiate the Write-One-Record instruction. The System Reset pulse (7-$\overline{\text{POR}}$) is also generated by the valid command clock to reset the tape transport controller to initial conditions. The Controller Busy flip-flop (7-$\overline{\text{CBUSY}}$) is set by the command clock to initiate the Write-One-Record instruction. The synchronous forward signal (7-$\overline{\text{SFC}}$) is sent to the tape unit to initiate forward motion.

After the Predelay (1-S1, S2) times out, the Submode 1 flip-flop (8-SM1) sets to control writing of the preamble. The Enable Write Data Request flip-flop(8-EWDR) then sets to allow the Data Flag flip-flop (16-DATA FLAG) to begin requesting write-data characters from the computer adapter. The 9-W/R ACK pulse from the computer adapter stores the character in the first stage of the Write storage register. At the next bit time, the character is shifted into the second stage of the Write storage register (to control the phase encoders) and then the Data Flag is set to request the next character. This process repeats until the computer adapter signals the end of the record with the 9-HALT signal, which resets 8-EWDR. The last character is then written and submode 2 flip-flop(8-SM2) is set to control writing the postamble.

For a single-gap tape unit, the Post Delay State 4 (1 -S4) is entered immediately after the postamble is written. For a dual-gap tape unit, the Post Delay is not entered until the delay counter times out after the last 17-IBG Pulse indicates that the read head has passed the end of the record (to allow parity-checking). At the end of the Post Delay, the Forward Motion signal is terminated (7-$\overline{\text{SFC}}$) and signal 5-$\overline{\text{DBY}}$ indicates that status may be checked and another Write command may be issued to continue without stopping in the IRG.

If "on-the-fly" writing is not attempted, the Halt Delay (1 -S5) times out while the tape is stopping in the IRG and the 7-$\overline{\text{CBUSY}}$ signal terminates to indicate that the Formatter is ready to accept the next command.

The timing diagram illustrates a single-gap case in which a two-character (0, 1) record is written. The 41-bit preamble and postamble are compressed to illustrate the important wave-forms. A negative-going transition of the Phase Encoded Data signal (5-WD_n) in the middle of a bit time defines a "zero" bit while a positive going transition defines a "one" bit. The Write Data Strobes (8-WDS) are at twice the bit-rate and are delayed slightly from the phase-encoded data transitions.

The phase encoded data wave-forms are generated by inverting the Bit-Rate Clock signal (2FCLK) during a bit cell for a "zero" and non-inverting for a "one".

Each data bit stored by the 9-$\overline{\text{W/R ACK}}$ pulse in the first stage Write storage buffer (in response to the Data Flag) is transferred to the second stage Write storage buffer at the next negative-going transition of the Bit Rate Clock (2-FCLK), where it controls the phase-encoding circuit for the next bit cell.

3.5.7 Read One Record (See Timing Diagram 3-9)

The Read One Record command is initiated when signal 9-SET RCC is high and the 9-STROBEC pulse occurs. The Valid Command pulse (6-VLD) clocks the 7-RCC flip-flop set in the command register. The system reset pulse (7-$\overline{\text{POR}}$) is generated by the 6-VLD clock to reset the Formatter to initial conditions. The Synchronous Forward command (7-$\overline{\text{SFC}}$) and the 7-$\overline{\text{CBUSY}}$ signal are activated at this time. After a Predelay (1 -S1, S2) interval (to allow the tape to get "up to speed"), the State Count Three (1 -S3) is set to enable the read logic.

At 1 -S3 time, the 5-$\overline{\text{DBY}}$ signal is activated.

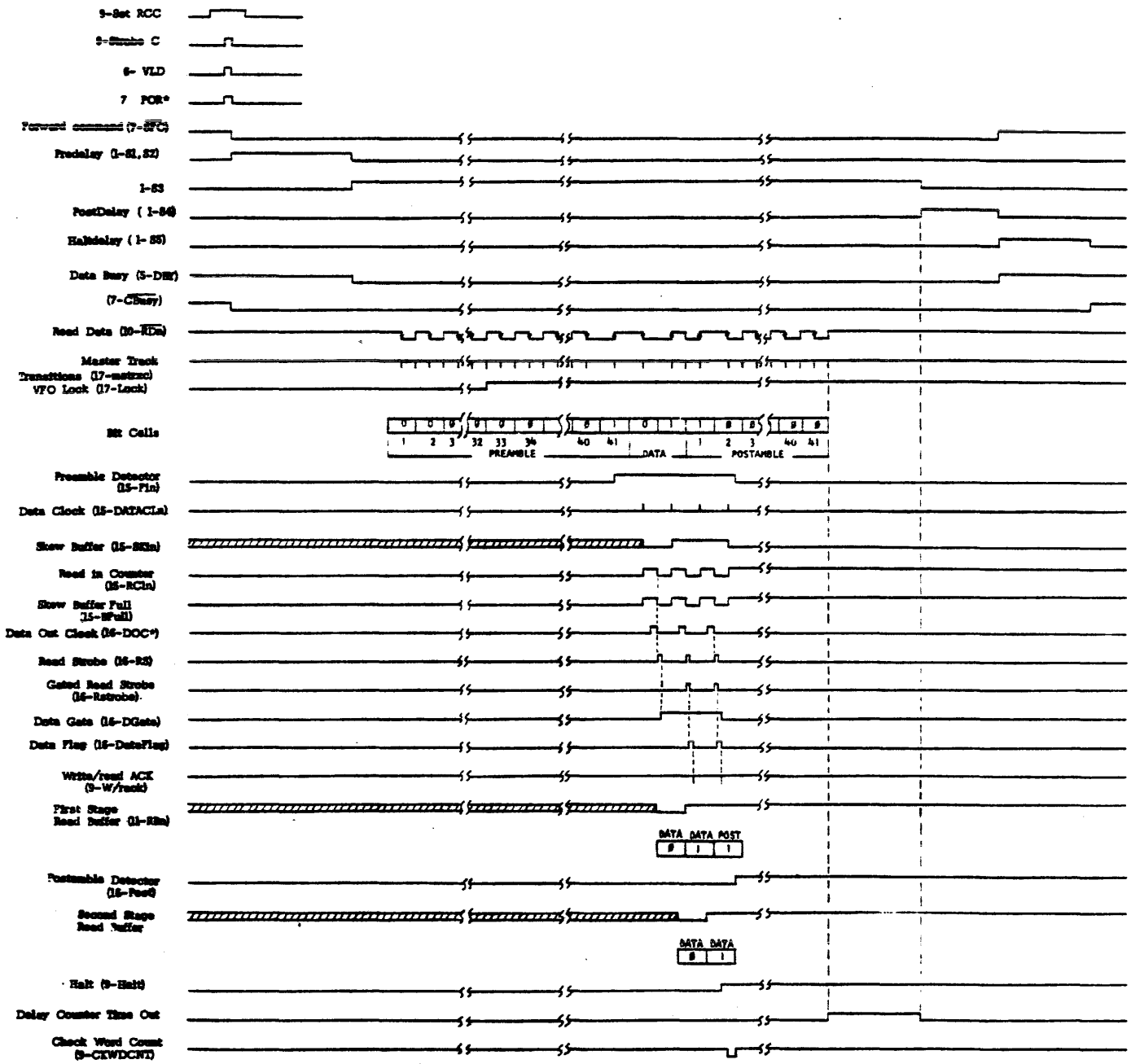


Figure 3-9. Read One Record Timing Diagram

When the master track transition pulses (17-MSTRXC) occur (indicating the start of the preamble), a counter begins counting to set the VFO Lock flip-flop (17-LOCK) at the 32nd bit of the preamble (the transitions occur at twice the bit rate in the preamble). Until the 17-LOCK flip-flop sets, the "window" counters for each track are resynced from every negative-going transition of the Read data.

The variable frequency oscillator (VFO) in the phase-locked-loop locks onto the bit rate from the "Master" track during the first 32 bits of the preamble. When the Formatter switches to the "lock" mode, the "window" counters on each track are assumed to be locked onto the "bit" transitions of the Read data and are utilized to ignore any "phase" transitions.

This is accomplished by developing a "window" that opens at 75% of the bit period and extends up to 125% of the bit period. Any transitions that occur within these "windows" are assumed to be the "bit" transition and are decoded to recover the Read data. They are used to reset the window counter for the next bit period. If the window counter extends beyond the 125% point without any data transition, a "drop-out" is detected, which sets the "Dead Track" flip-flop for the track in which the drop-out occurred.

The window counters operate from the output of the VFO divided by two. Since the VFO operates at thirty-two times the bit rate, the window counters divide each bit period into 16 increments. Therefore, ±4 increments around the count of 16 is allowed for the "window".

When the "all ones" character at the end of the preamble is sensed in each track, the Preamble Detector flip-flop ($15\text{-}FI_n$) sets to enable the Data clock ($15\text{-}DATACL_n$) for the particular track. At the bit-transition in the middle of the first data bit cell, the Data clock shifts the decoded data bit into the first stage of the four-bit skew buffer register and clocks the Read-In Counter ($15\text{-}RCI_n$) from a count of zero to a count of one.

When all of the nine Read-In Counters have been advanced from the "empty" count of zero, the Skew Buffer Full (15-BFULL) signal is activated.

NOTE: The timing diagram is drawn for a single track only, hence assumes that the other Read-In Counters have already advanced off zero such that this track is the "latest" one. Therefore, 15-BFULL follows this track's RCI signal.

A Data-Out Clock pulse (15-DOC*) is then generated to shift all Read-In Counters backward one count and shift the assembled character out of the nine skew-buffer registers into the first stage of the two-stage read buffer register (this terminates the 15-BFULL signal).

A read strobe pulse (16-RS) is generated after the trailing edge of the Data Out clock. The trailing edge of the first RS pulse sets the data gate flip-flop (10-DGATE) to enable the succeeding RS pulses to operate the Data Flag flip-flop and to be output to the computer adapter for strobing the contents of the second stage of the Read buffer register.

The "Read-In Counter - Buffer Full - Data Out Clock - Read Strobe" sequence is repeated for all following characters until the postamble is detected by sensing an "all ones" character in the first stage of the read buffer and an "all zeroes" character present at the outputs of the skew buffers. This disables the Data Out clock to halt the sequence.

The leading edge of the second Data Out clock transfers the first data character from the first to the second stage of the Read buffer such that the data will be settled by the time the RS pulse is generated.

The gated Read strobe(16.RSTROBE) is then generated to the computer adapter interface for the first data character and the 16-data flag is set to request transfer.

When the computer adapter responds with a 9-$\overline{\text{W/R ACK}}$ pulse, the data flag is reset.

The leading edge of the gated Read strobe can be utilized by the computer adapter to toggle a binary flip-flop in the computer adapter if "packing" of it is desired to pack more than one tape character into a single word for transfer to the computer.

This insures that the toggled binary will be settled by the time that the Data Flag is set, so that the Toggle flip-flop can be gated with the Data Flag signal. This "forces" a 9-$\overline{\text{W/R ACK}}$ pulse for those tape characters collected by the computer adapter before an actual transfer to the computer is initiated.

The toggle flip-flop can then be checked at pulse 9-$\overline{\text{CKWDCNT}}$ time to detect an odd number of characters in the record. This too "forces" a data transfer to the computer for the extra "odd" character, since Packing logic normally expects an even number of characters and a data transfer to the computer normally occurs after every even character.

There is a built-in delay from the 9-$\overline{\text{W/R ACK}}$ pulse to direct-reset of the Data Flag such that this utilization of the Data Flag signal to reset itself is acceptable.

When the actual computer transfer is requested, pulse 9-$\overline{\text{W/R ACK}}$ should be derived from the computer acceptance of the transfer, so that a data transfer failure can be detected by the Formatter.

When the last transfer required is requested, the computer adapter should generate the 9-HALT signal, which terminates the 16-DGATE, hence the 16-DATA Flag signals (even if there are more characters in the record).

When the postamble is detected, the Preamble Detection flip-flops are reset in all tracks to "strip off" the postamble by disabling further data clocks. The check and count pulse (9-$\overline{\text{CKWDCNT}}$) is also generated so that, when packing data, the computer adapter can force an extra data transfer (if there were an odd number of characters in the record) and can determine if the record was shorter or longer than expected.

After the last master track transitions occur, the Delay Counter begins timing out, then switches the Formatter to the Post Delay State (1 -S4). After the Post Delay times out, the Synchronous Forward command (7-$\overline{\text{SFC}}$) is terminated, the Halt Delay State (1 -S5) is entered and the Data Busy signal (5-$\overline{\text{DBY}}$) is terminated.

The transport begins "ramping" down to a halt in the inter-record gap.

When the Halt Delay interval is past, the transport is stopped in the gap and the 7-$\overline{\text{CBUSY}}$ signal is terminated to indicate that the Formatter is ready to accept the next command.

If another Read operation in the same direction is to occur, the status may be read after signal 5-DBY terminates and the next Read command issued immediately to accomplish non-stop operation. This halves the amount of time required to traverse the inter-record gap.

3.5.8 Erase 3-Inch Gap

The Erase-3-Inch-Gap timing is similar to the Write-File-Mark timing except 1 -S2 generates the Predelay and no writing occurs.

3.6 CONTINUOUS WRITE OR READ

Continuous Write allows the IRG to be generated at full rated tape speed. If successive write commands are based upon the termination of the CBUSY command (as is normal) then the tape comes to a full stop in the IRG.

Similarly, Continuous Read (or Space) allows the IRG to be traversed at full rated tape speed.

This mode of operation optimizes the usage of the tape units by minimizing the amount of "dead time" where-in data transfer cannot take place in the IRG. In order to obtain continuous "on-the-fly" operation, the DBY signal may be used (instead of the CBUSY signal) as long as the following restrictions are met:

1. The next command may not switch from a Read to a Write mode (or vice versa).
2. The next command may not switch tape direction.
3. A Rewind or Offline command may not follow a Write or Write-File-Mark command.

A Write or Write-File-Mark command can follow a Write or Write-File-Mark command as soon as signal DBY terminates, rather than waiting until signal DBY terminates.

Similarly, a Read or Space Forward command can follow the same type command upon termination of DBY.

A Read or Space Reverse command can follow the same type command upon termination of DBY.

3.7 OPTIONS

The following field-changeable options are provided-for in the Formatter:

1. Selection of two different tape speeds.
2. Definition of which tape units are single-stack (read/write) and which ones are dual-stack (read-after-write).

3.7.1 Tape Speed

The tape speed selection option provides control over the "Speed Clock" and the "Write Clock" divider chains that operate from the crystal oscillators. There can be two different tape speeds selected. The selection is accomplished by controlling the division modulo of a flip-flop divider chain by loading the negative two's-complement of the desired (divisor-1) whereupon the counter counts up to zero to recycle.

Chip position D28 on card assembly number 76191 is provided as a plug-in wire-wrap socket for this purpose. Input Pins 1, 2, 3 and 4 represent the four tape units A, B, C and D respectively. All tape units at speed #1 must have their "input" pins bussed together (call this BUS #1) and all tape units at speed #2 must have their input pins bussed together (call this BUS #2).

Bus #1 must then be jumpered to Field #1 pins 5, 6, 7, 8 and 9 as indicated in Table 3-2 to obtain the desired division ratio. Similarly, Bus #2 must be jumpered to Field #2 pins 11, 12, 13, 14, and 15 as indicated in Table 3-2 to obtain the second desired division ratio.

Table 3-2. Tape Speed Selection

Col 1	Col 2	Col 3	Col 4						Col 5	Col 6
Tape Speed	Division Ratio	NEG. 2's Complement	16	8	4	2	1	←BINARY BIT WT.	SPDCLK FREQ kHz (PIN A29-12)	WRITE CLOCK FREQ kHz (PIN E-319)
			9	8	7	6	5	←FIELD #1 PINS (D28)		
			15	14	13	12	11	←FIELD #2 PINS (D28)		
112.5	2	-1	0	1	1	1	1		22.5	360
75	3	-2	0	1	1	1	0		15	240
56.25	4	-3	0	1	1	0	1			
45	5	-4	0	1	1	0	0		9	144
37.5	6	-5	0	1	0	1	1		7.5	120
32.14	7	-6	0	1	0	1	0			
28.125	8	-7	0	1	0	0	1			
25	9	-8	0	1	0	0	0		5	80
22.5	10	-9	0	0	1	1	1			
20.45	11	-10	0	0	1	1	0			
18.75	12	-11	0	0	1	0	1			
17.3	13	-12	0	0	1	0	0			
16.07	14	-13	0	0	0	1	1			
15.0	15	-14	0	0	0	1	0			
14.06	16	-15	0	0	0	0	1			
13.23	17	-16	0	0	0	0	0			
12.5	18	-17	1	1	1	1	1		2.5	40
11.84	19	-18	1	1	1	1	0			
11.25	20	-19	1	1	1	0	1			
10.7	21	-20	1	1	1	0	0			
10.22	22	-21	1	1	0	1	1			
9.7	23	-22	1	1	0	1	0			
9.38	24	-23	1	1	0	0	1			
9.0	25	-24	1	1	0	0	0			
8.6	26	-25	1	0	1	1	1			
8.3	27	-26	1	0	1	1	0			
8.03	28	-27	1	0	1	0	1			
7.77	29	-28	1	0	1	0	0			
7.5	30	-29	1	0	0	1	1			
7.2	31	-30	1	0	0	1	0			
7.03	32	-31	1	0	0	0	1			

NOTES:

1. In Col 4, pins marked "0" must be jumpered to Bus #1 or #2, pins marked "1" must be jumpered to Pin 16 to enable.
2. Standard tape speeds are underlined.
3. Jumper pin 10 to Bus representing tape speed of 37.5 ips or faster.

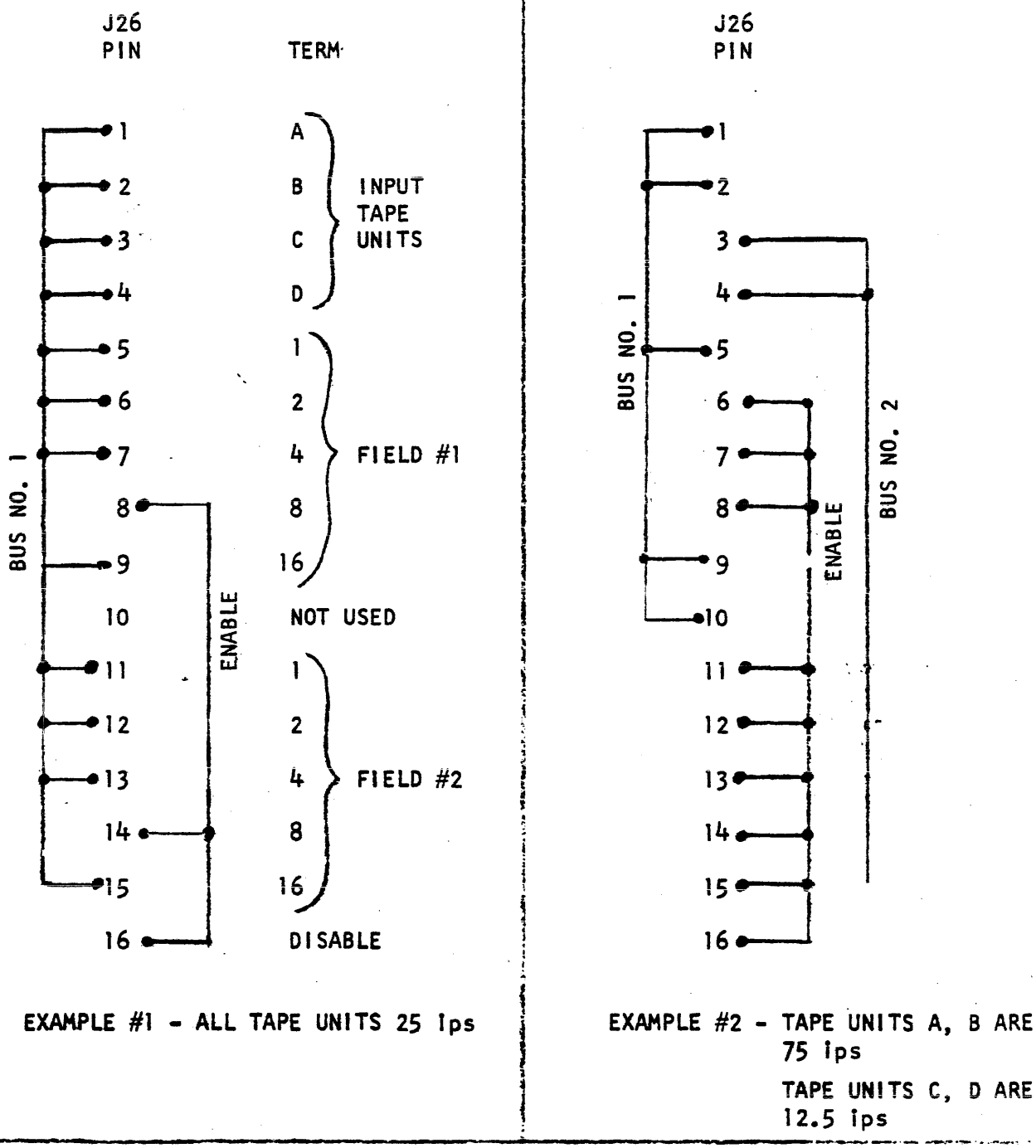


Figure 3-10. Example Tape Speed Selection

Figure 3-10 illustrates two examples of jumper wiring of socket D28 to achieve the desired tape speeds.

All remaining pins in Fields #1 and #3 must be jumpered to pin 16 to disable them. Note in the table that column 5 gives the frequency of the "Speed Clock" utilized by the delay counter for time interval calculation. Note also that column 6 gives the write clock frequency for the standard tape speeds.

Pin 10 must be jumpered to either (or both) Bus #1 or Bus #2 if they represent tape speeds of 37.5 ips or greater.

3.7.2 Single/Dual Stack Head Selection

The Formatter is configured so that if no jumpers are used in the SS/DS Head Selection Field then Dual Stack (read-after-write) is assumed.

Jumpers must be used only for the tape units A, B, C, or D that are single-stack head units.

The SS/DS Head Selection Field is located on assembly number 76191 near chip position B29. B29-9, 11, 12, 14, must be jumpered to points B29-6, 4, 3, or B29-1 for single-stack tape units A, B, C or D respectively.

3.7.3 Rewind Interrupt

The Formatter is configured to set CBUSY when the Rewind command is issued if no jumper is present between E8 and E9 (near M27). resets when the rewind is complete to provide a signal to the computer to indicate that the next command can be accepted.

If the jumper is present, CBUSY will not set for a rewind command. See Logic 7.

3.7.4 Formatter Address Select (See Logic 9

The Formatter is configured to always be selected if no jumper is placed in the Formatter Address Select area. Thus, if a single Formatter is utilized, no jumper need be used.

Table 3.3 illustrates the jumper connection required for the two addresses. The E points are located near row 32 on assembly 76193.

Table 3.3. Formatter Address Selection (Assy. 76193)

Formatter Address	Signal $\overline{\text{FAD1}}$	Jumper	
0	High	E1	E3
1	Low	E2	E3

3.8 DELAY TIMES

There are three main delay times:

1. Predelay
2. Postdelay
3. Halt Delay

The Pre/Post delays are used to erase portions of the Inter-Record Gap (when writing) or to erase tape. When reading they are used to position the head correctly in the IRG so that the following record can be either a read or a write.

The Halt delay is also used to erase part of the IRG when writing, and provides sufficient time to insure that the tape unit is completely stopped (after the motion signal is terminated).

There are many factors that enter into the various delays:

1. Tape speed
2. Single/dual-stack head
3. Forward/reverse motion
4. BOT/$\overline{\text{BOT}}$
5. Write/read command
6. EDIT/$\overline{\text{EDIT}}$ mode

Tables 3-9 through 3-13 give the delay times for a 9-track tape unit selected at the standard speeds of 75, 45, 37.5, 25, and 12.5 ips.

Table 3-4. NINE TRACK PRE/POST DELAYS (75 ips)

		PREDELAY				Time Interval Milliseconds	POSTDELAY				Time Interval Milliseconds
		FROM		TO			FROM		TO		
		Signal	Pin	Signal	Pin						
Single Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	3.66	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	1.67
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	12.0	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	1.67
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	3.66	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	0
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	3.66	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	.33
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	53.6	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	2.66
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65	5.66	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	2.66
Dual Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	3.66	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	0
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	12.0	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	0
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	3.66	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	1.67
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	3.66	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	2.33
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	53.6	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	.33
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65	5.66	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	.33

HALTDELAY				
FROM		TO		
$\overline{DBY}$(1)	J101-65	CBUSY(1)	J101-94	5.66

NOTES
1. Read = Read 1 record or space
2. Write = Write 1 record or write file mark
3. (transition) = 0 means from +5V to 0V, = 1 means from 0V to +5V

Table 3.5. NINE TRACK PRE/POST DELAYS (45 ips)

		PREDELAY				Time Interval Milliseconds	POSTDELAY				Time Interval Milliseconds
		FROM		TO			FROM		TO		
		Signal	Pin	Signal	Pin						
Single Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	6.08	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	2.78
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	19.9	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	2.78
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	6.08	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	0
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	6.08	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	.54
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	89.0	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	4.4
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65	9.4	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	4.4
Dual Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	6.08	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	0
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	19.9	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	0
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	6.08	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	2.78
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	6.08	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	3.86
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	89.0	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	.54
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65	9.4	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	.54

HALTDELAY				
FROM		TO		
$\overline{DBY}$(1)	J101-65	CBUSY(1)	J101-94	9.4

NOTES
1. Read = Read 1 record or space
2. Write = Write 1 record or write file mark
3. (transition) = 0 means from +5V to 0V, = 1 means from 0V to +5V

Table 3.6. NINE TRACK PRE/POST DELAYS (37.5 ips)

		PREDELAY				Time Interval Milliseconds	POSTDELAY				Time Interval Milliseconds
		FROM		TO			FROM		TO		
		Signal	Pin	Signal	Pin						
Single Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	7.3	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	3.34
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	24.0	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	3.34
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	7.3	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	0
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	7.3	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	.66
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	107.3	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	5.3
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65	11.3	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	5.3
Dual Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	7.3	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	0
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	24.0	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	.0
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	7.3	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	3.34
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	7.3	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	4.64
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	107.3	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	.66
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65	11.3	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	.66

HALTDELAY			
FROM		TO	
$\overline{DBY}$(1)	J101-65	CBUSY(1)	J101-94

11.3

NOTES
1. Read = Read 1 record or space
2. Write = Write 1 record or write file mark
3. (transition) = 0 means from +5V to 0V, = 1 means from 0V to +5V

Table 3.7. NINE TRACK PRE/POST DELAYS (25 ips)

		PREDELAY				Time Interval Milliseconds	POSTDELAY				Time Interval Milliseconds
		FROM		TO			FROM		TO		
		Signal	Pin	Signal	Pin						
Single Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	11	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	5
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	36	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	5
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	11	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	0
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	11	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	1
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	161	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	8
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65	17	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	8
Dual Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	11	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	0
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	36	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	0
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	11	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	5
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	11	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	7
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	161	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	1
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65	17	$\overline{S3}$(1)	E3	$\overline{DBY}$(1)	J101-65	1

HALTDELAY				
FROM		TO		
$\overline{DBY}$(1)	J101-65	CBUSY(1)	J101-94	17

NOTES
1. Read = Read 1 record or space
2. Write = Write 1 record or write file mark
3. (transition) = 0 means from +5V to 0V, = 1 means from 0V to +5V

Table 3.8. NINE TRACK PRE/POST DELAYS (12.5 ips)

		PREDELAY				Time Interval Milliseconds	POSTDELAY		Time Interval Milliseconds
		FROM		TO			FROM	TO	
		Signal	Pin	Signal	Pin				
Single Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	22	$\overline{S3}$(1) E3	$\overline{DBY}$(1) J101-65	10
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	72	$\overline{S3}$(1) E3	$\overline{DBY}$(1) J101-65	10
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	22	$\overline{S3}$(1) E3	$\overline{DBY}$(1) J101-65	0
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	22	$\overline{S3}$(1) E3	$\overline{DBY}$(1) J101-65	2
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	322	$\overline{S3}$(1) E3	$\overline{DBY}$(1) J101-65	16
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65	34	$\overline{S3}$(1) E3	$\overline{DBY}$(1) J101-65	16
Dual Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	22	$\overline{S3}$(1) E3	$\overline{DBY}$(1) J101-65	0
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	72	$\overline{S3}$(1) E3	$\overline{DBY}$(1) J101-65	0
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	22	$\overline{S3}$(1) E3	$\overline{DBY}$(1) J101-65	10
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	22	$\overline{S3}$(1) E3	$\overline{DBY}$(1) J101-65	14
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	322	$\overline{S3}$(1) E3	$\overline{DBY}$(1) J101-65	2
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65	34	$\overline{S3}$(1) E3	$\overline{DBY}$(1) J101-65	2

HALTDELAY		
FROM	TO	
$\overline{DBY}$(1) J101-65	CBUSY(1) J101-94	34

NOTES
1. Read = Read 1 record or space
2. Write = Write 1 record or write file mark
3. (transition) = 0 means from +5V to 0V, = 1 means from 0V to +5V

SECTION IV

DRAWINGS

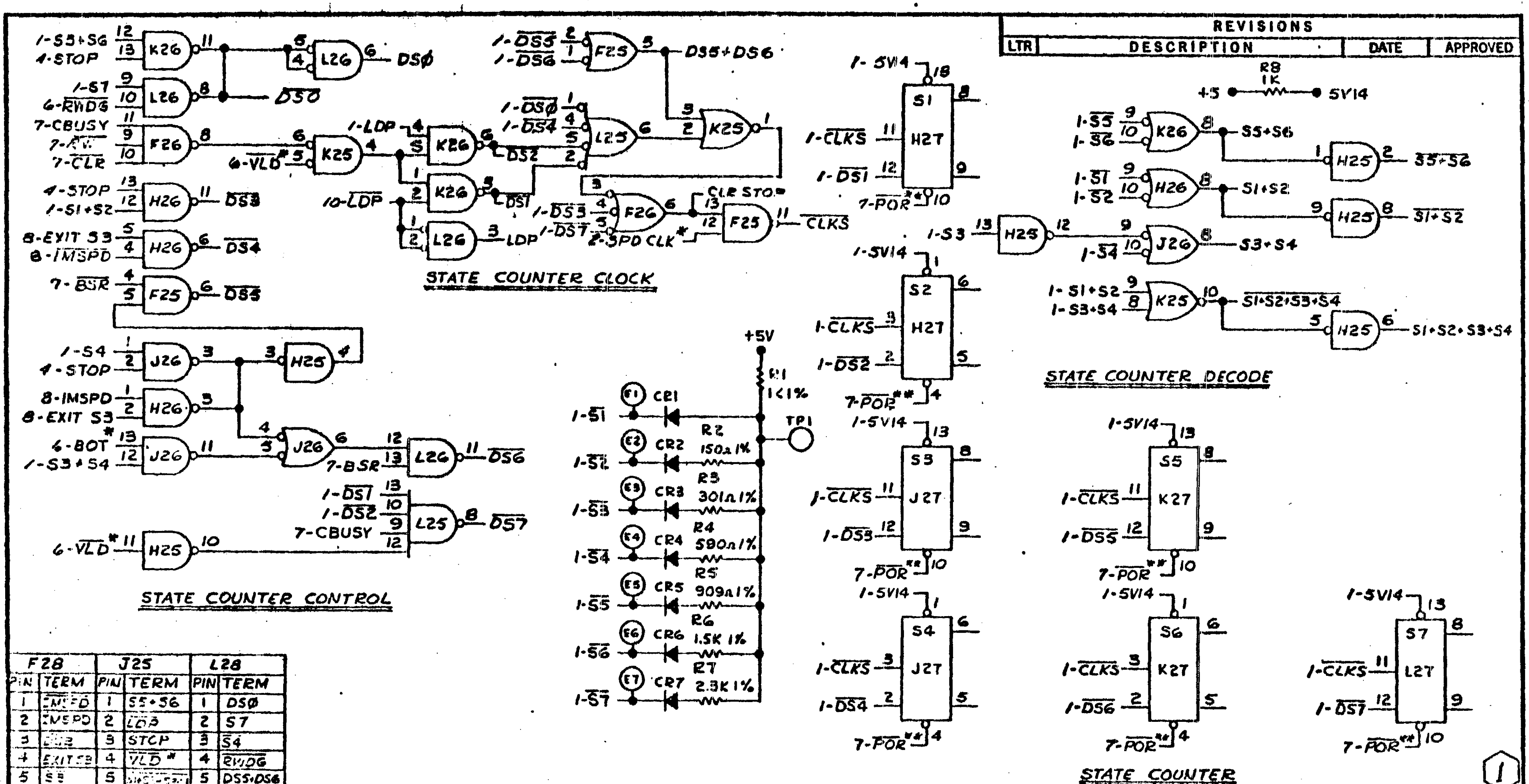
(By Logic Number)

Logic 1	State Counter
Logic 2	Oscillator Board
Logic 2A	Oscillator Board
Logic 3	Write Logic (Write Reg's & Partiy Gen)
Logic 4	Write Logic (Delay Counter
Logic 5	Write Logic (Write Phase Encoders)
Logic 6	Write Control (Reject, Status, Select)
Logic 7	Write Control (Command Reg, Xport Control) (Busy)
Logic 8	Write Control
Logic 9	Write Control (Computer Adapter Interface)
Logic 10	Write Control (Transport Interface)
Logic 11	Read Logic (Read Reg's & Postamble Detect)
Logic 12	Read Logic (Parity Check)
Logic 13	Dead Track Detector
Logic 14	Voltage Control Oscillator
Logic 15	Read Logic (Skew Buffer Deadtrack & Window Counter) (3 Sheets)
Logic 16	Read Control
Logic 17	Read Control

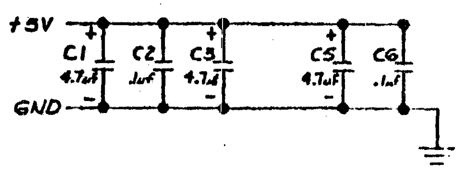
Assy : Read Logic 76142
Dead Track Detector 76180
Read Logic 76181
Read Control 76182
Voltage Control Oscillator 76183
State Counter 76190
Oscillator Board 76191

DRAWINGS Cont

Write Logic 76192
Write Control 76193 (2 sheets)
Power Supply 940047 (3 sheets)
Power Supply 1080000
Power Supply 1080500



F28		J25		L28	
PIN	TERM	PIN	TERM	PIN	TERM
1	IMSPD	1	S5+S6	1	DSØ
2	IMSPD	2	LDP	2	S7
3	[illegible]	3	STOP	3	S4
4	EXIT S3	4	VLD *	4	RWDG
5	S3	5	[illegible]	5	DS5+DS6
6	POR **	6	S1+S2	6	N.C.
7	S2	7	GND	7	GND
8	CBUSY	8	S3+S4	8	S2
9	RW	9	[illegible]	9	S3
10	CLR	10	S1+S2+S3+S4	10	S4
11	[illegible]	11	BOT *	11	S6
12	CLR STOP	12	BSR	12	S1
13	SPD CLK *	13	S5+S6	13	S5
14	+5V	14	+5V	14	N.C.



DIETZGEN 156 MG 10

4-18-72

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TITLE STATE COUNTER

DWN S. RIZUTO 6/3/71

CHK

ENGR

SCALE

FSC 31160

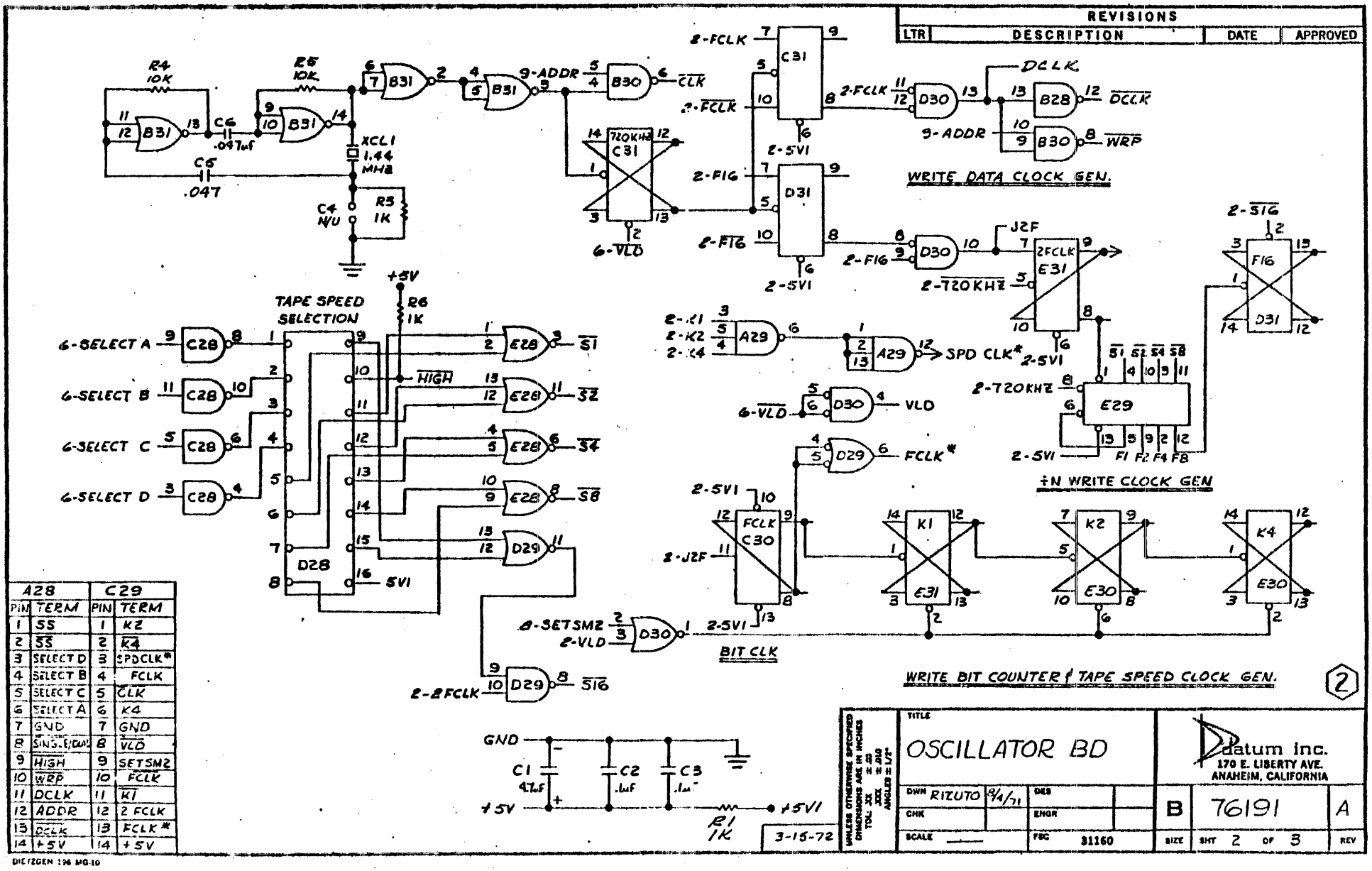
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

SIZE B 76190

SHT 2 OF 2

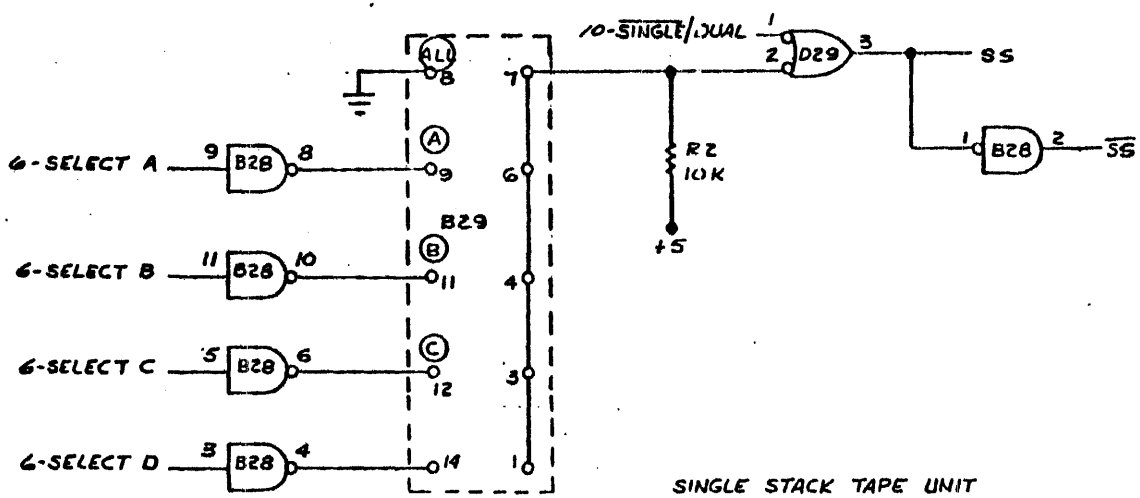
REV

(1)



A28		C29	
PIN	TERM	PIN	TERM
1	S5	1	K2
2	$\overline{S5}$	2	$\overline{K4}$
3	SELECT D	3	SPDCLK*
4	SELECT B	4	FCLK
5	SELECT C	5	$\overline{CLK}$
6	SELECT A	6	K4
7	GND	7	GND
8	SNS.E/OW	8	$\overline{VLD}$
9	HIGH	9	SETSM2
10	$\overline{WRP}$	10	FCLK
11	DCLK	11	$\overline{K1}$
12	ADDR	12	2 FCLK
13	DCLK*	13	FCLK*
14	+5V	14	+5V

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

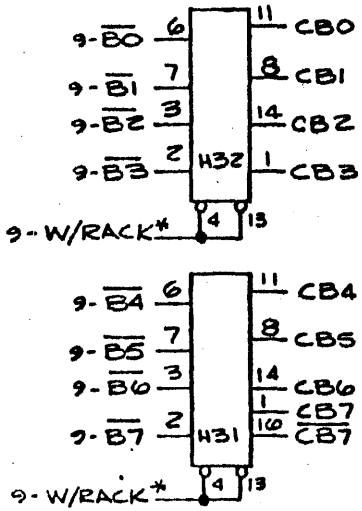


SINGLE STACK TAPE UNIT SELECTION

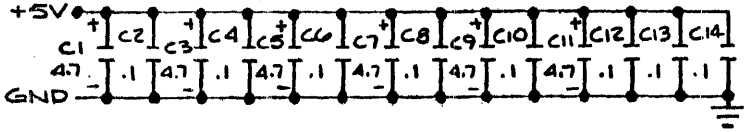
2a

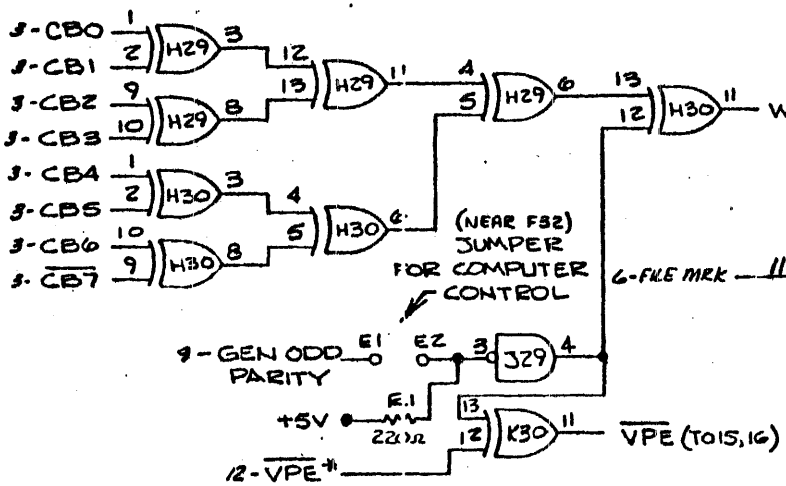
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ± .03 .XXX ± .010 ANGLES ± 1/2°	TITLE: OSCILLATOR BD.			datum inc. 170 E. LIBERTY AVE. ANAHEIM, CALIFORNIA	
	DWN RIZUTO	8/6/71	DES	B	76191 A
	CHK		ENGR		
3-15-72	SCALE —		FSC 31160	SIZE	SHT 3 OF 3 REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

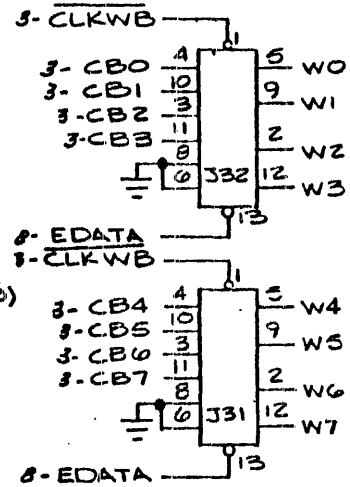


WRITE STORAGE REGISTER A

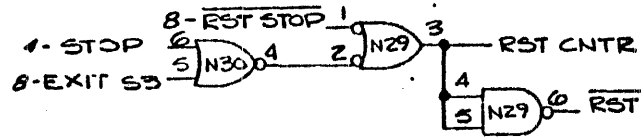




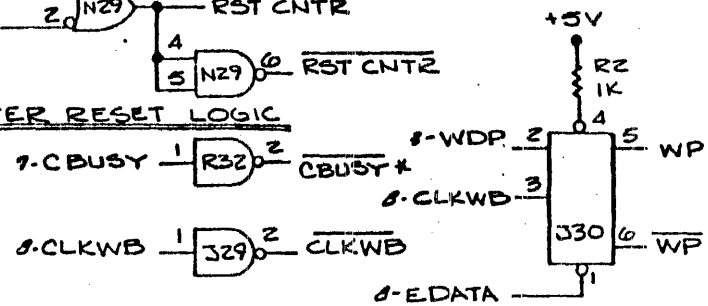
WRITE ODD PARITY GENERATOR



WRITE STORAGE REGISTER B



COUNTER RESET LOGIC

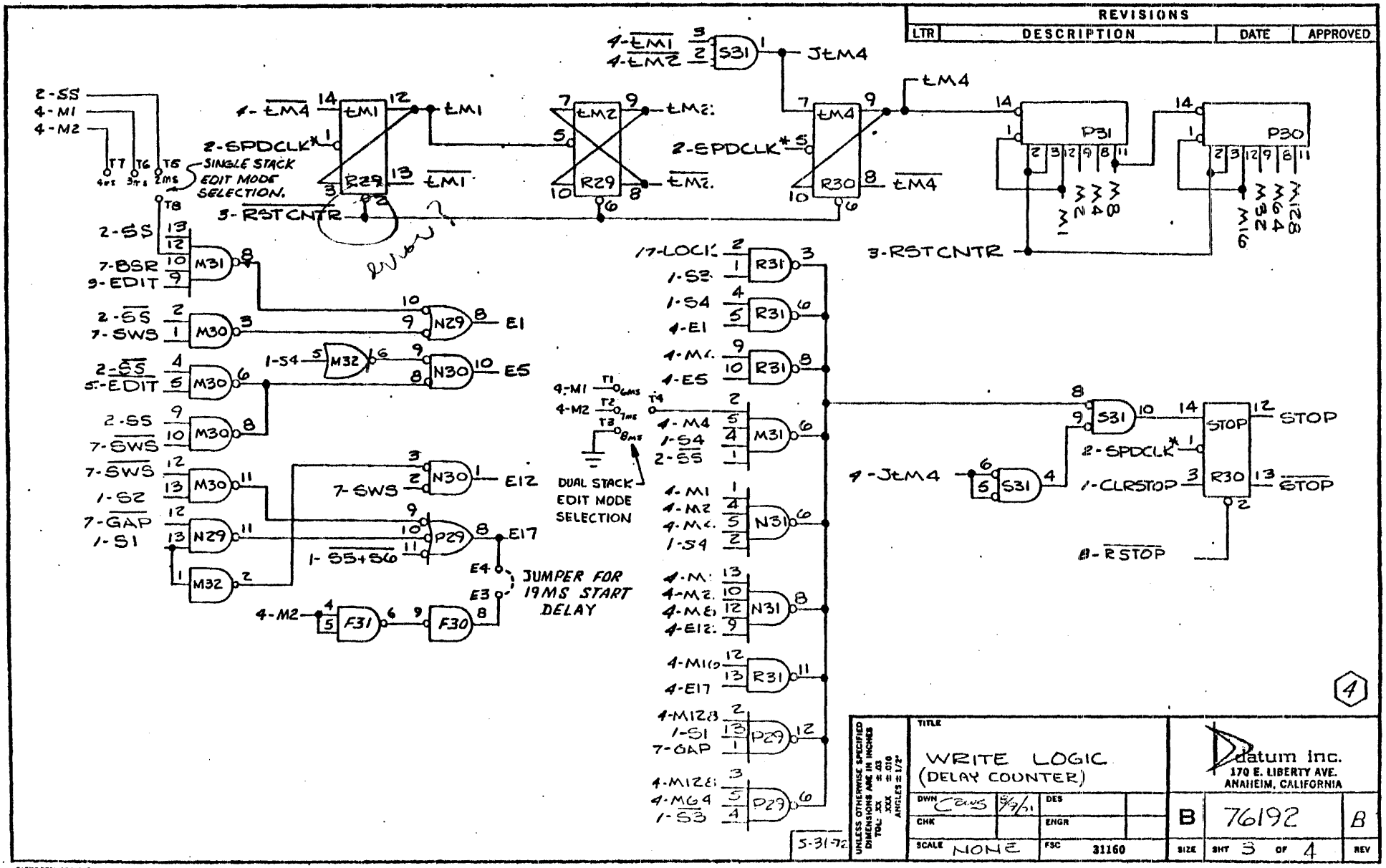


F29		M29		P32		F32		N32		S29	
PIN	TERM	PIN	TERM	PIN	TERM	PIN	TERM	PIN	TERM	PIN	TERM
1	S3	1	VPE	1	CBUSY	1	B3	1	WDP	1	SPDCLK*
2	EXIT S3	2	S4	2	EDIT	2	B2	2	I-S1	2	JAM4
3	LDP	3	BAR	3	M16	3	W/RACK*	3	FPT	3	GAP
4	THR1	4	S5+S6	4	EDIT	4	FM	4	FPT	4	EDATA
5	THR2	5	S3	5	THR1	5	ADDR	5	LDP	5	CLR STOP
6	RDY	6	SWS	6	ADDR	6	B0	6	RDY	6	STOP
7	GND	7	GND	7	THR2	7	B1	7	S26-8	7	GND
8	S3+S4	8	S2	8	WD6	8	CBUSY*	8	WD1	8	H23-6
9	DET	9	SWS	9	WD5	9	9TRK	9	WD5	9	STOP
10	CD3	10	S3	10	M128	10	GEN ODD PARITY	10	VPE*	10	S4
11	N.C.	11	EDIT	11	WD7	11	B5	11	WD3	11	LOCK
12	FORM REJECT	12	GAP	12	WRITE*	12	B4	12	WD2	12	1ST STOP
13	B32-3	13	CLK WB	13	SWS	13	B6	13	P24-10	13	S3
14	+5V	14	+5V	14	M1	14	B7	14	WD4	14	+5V

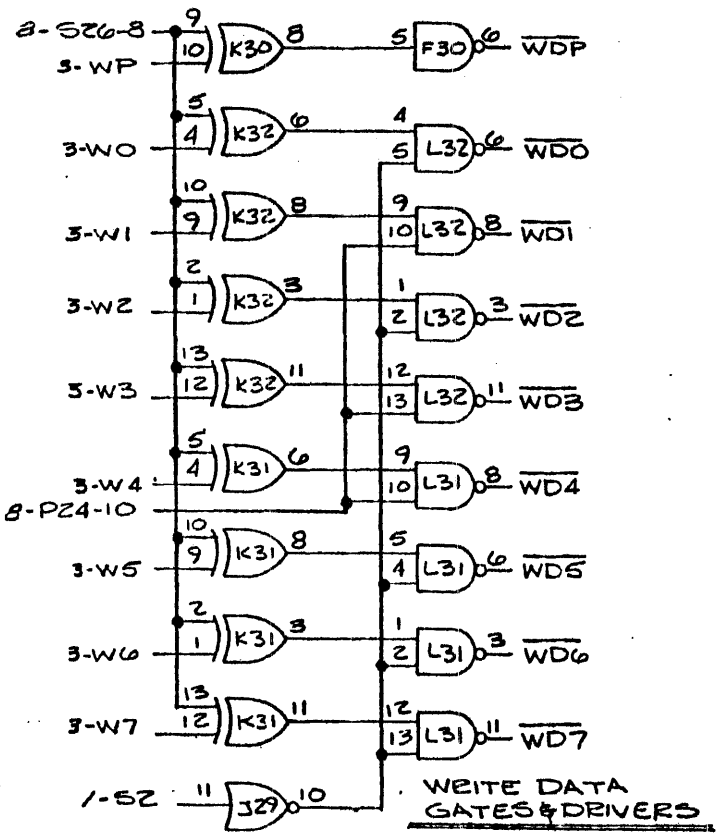
3

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: XX = .03, XXX = .010, ANGLES = 1/2°	TITLE: WRITE LOGIC (WRITE REG'S & PARITY GEN)	datum inc. 170 E. LIBERTY AVE. ANAHEIM, CALIFORNIA			
S-31-72	DWN Cook 5/6/71	DES	B	76192	B
	CHK	ENGR			
	SCALE NONE	FSC 31160	SIZE	SHT 2 OF 4	REV

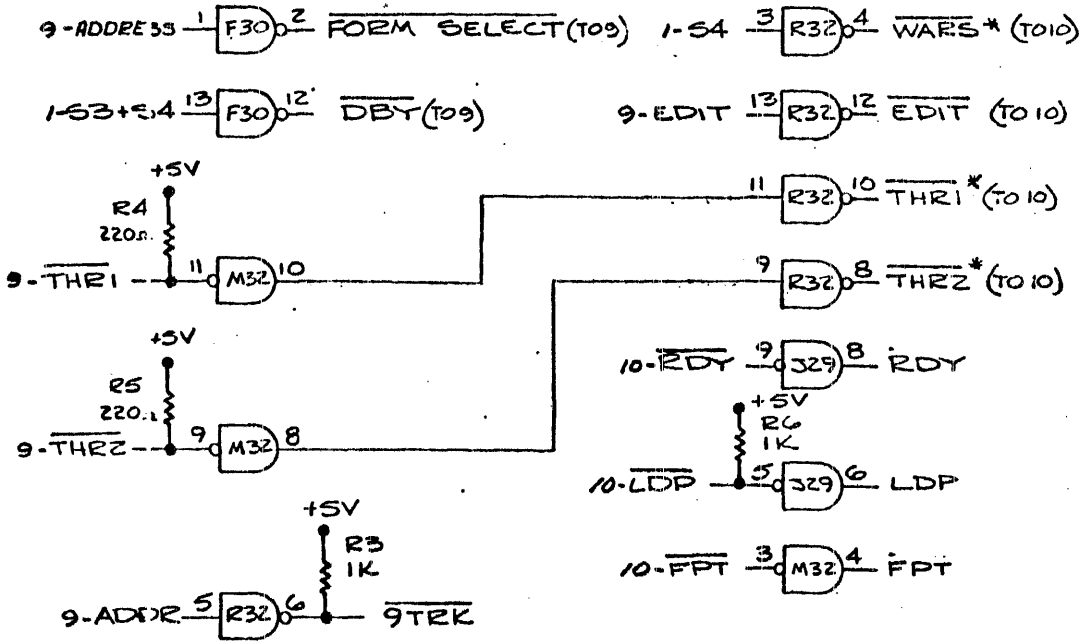
DIETZGEN 196 MG 10



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

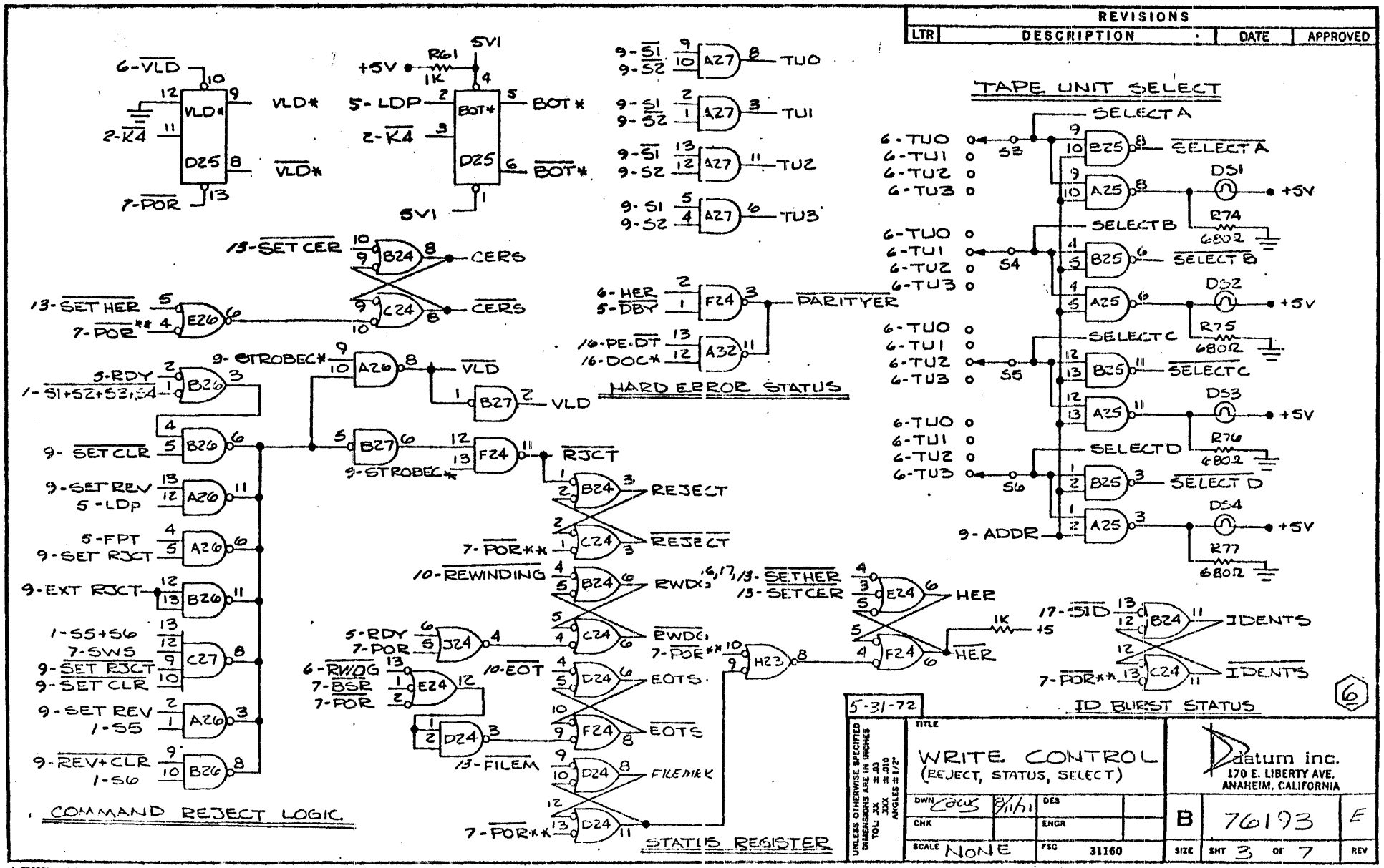


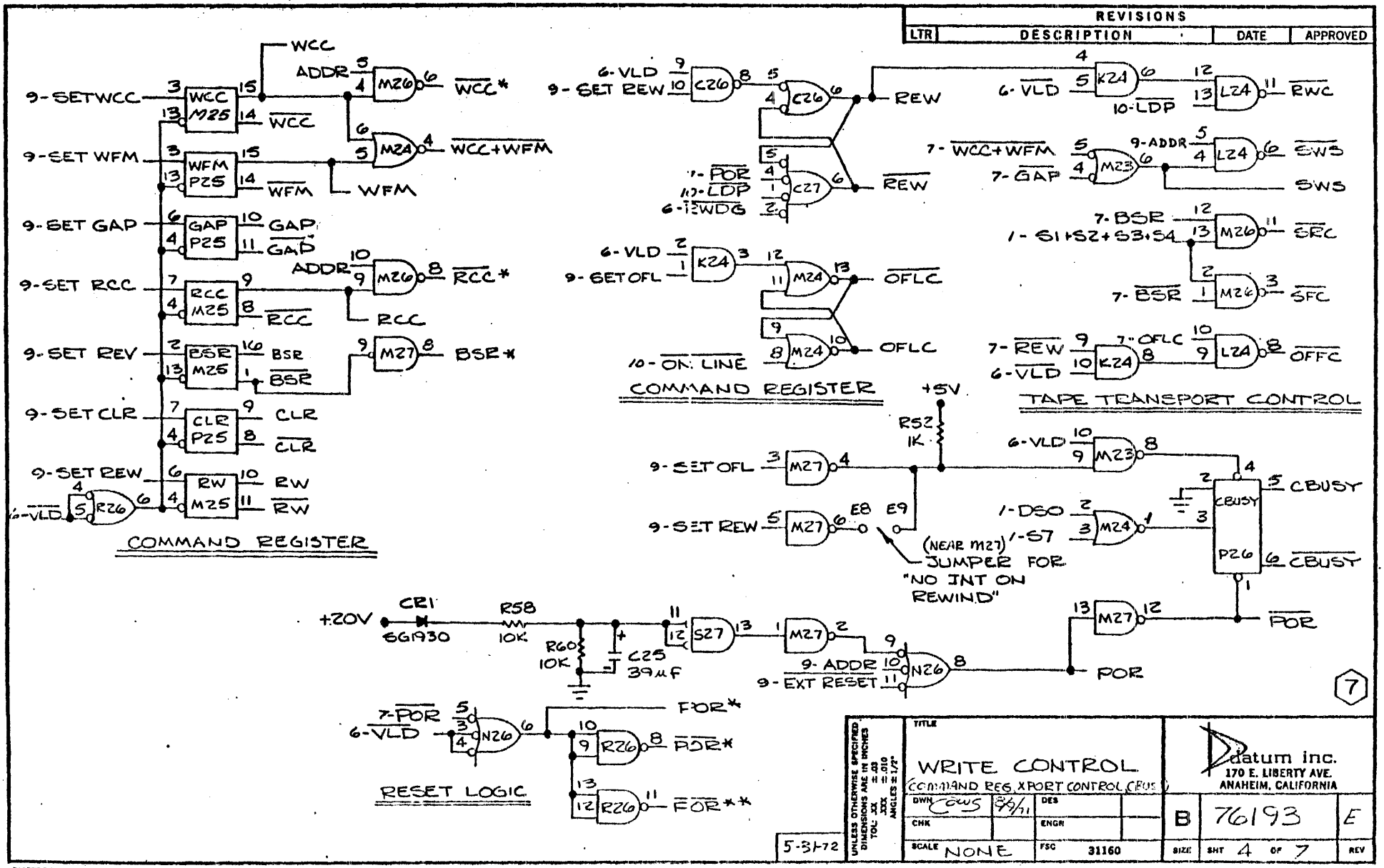
⊕ PHASE ENCODERS. (OUTPUTS ARE FCLK FOR ZERO, $\overline{FCLK}$ FOR ONE)

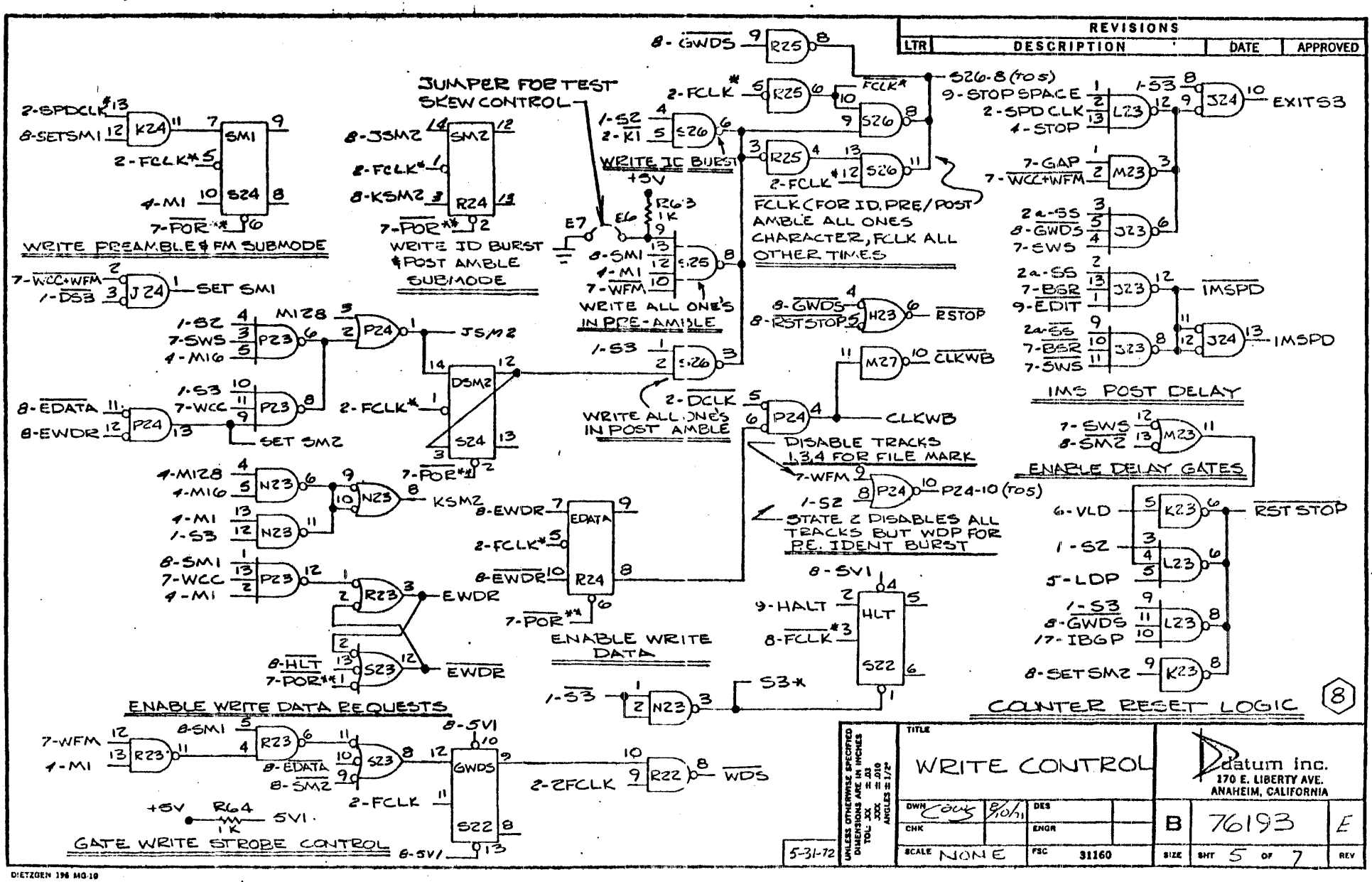


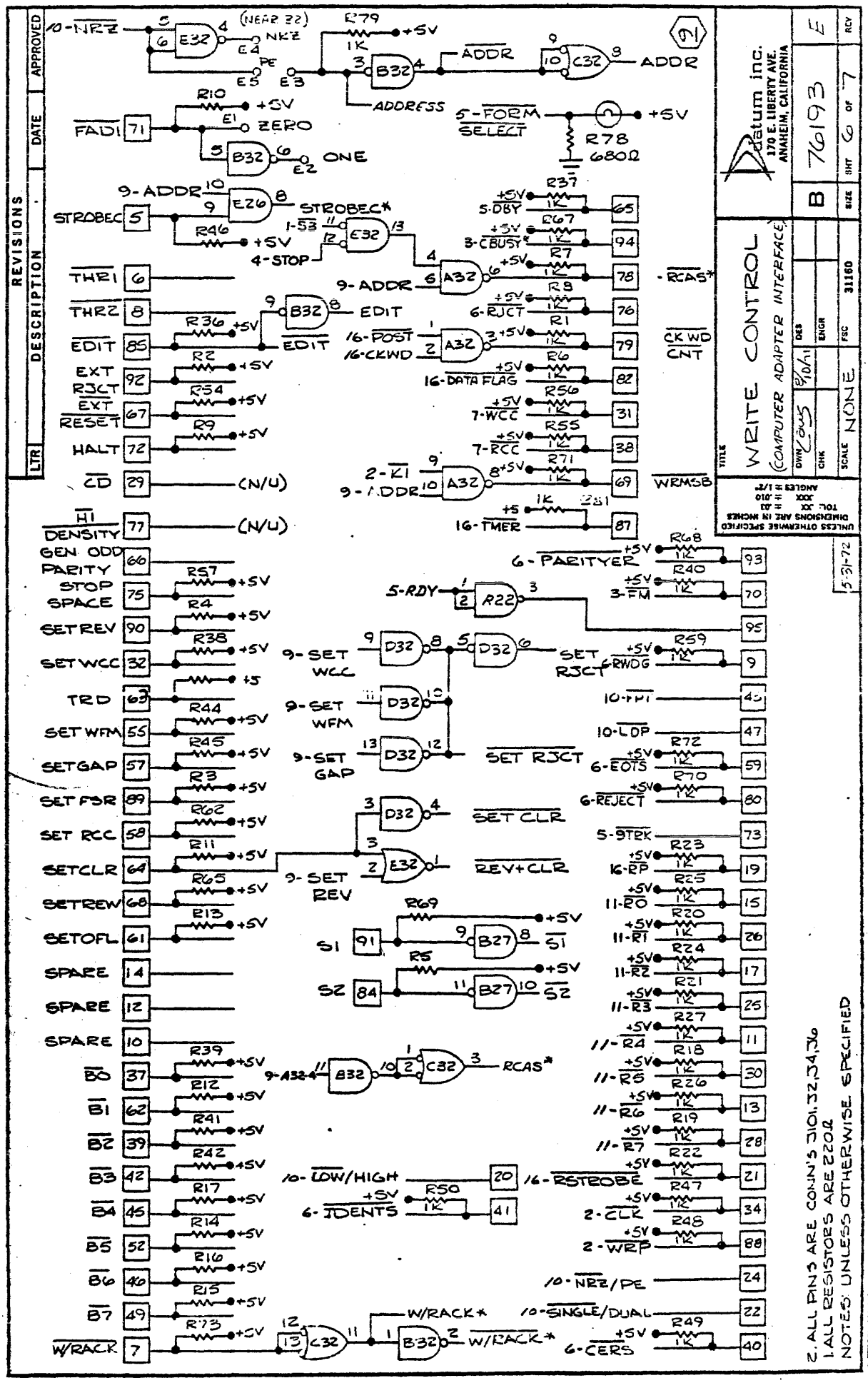
5

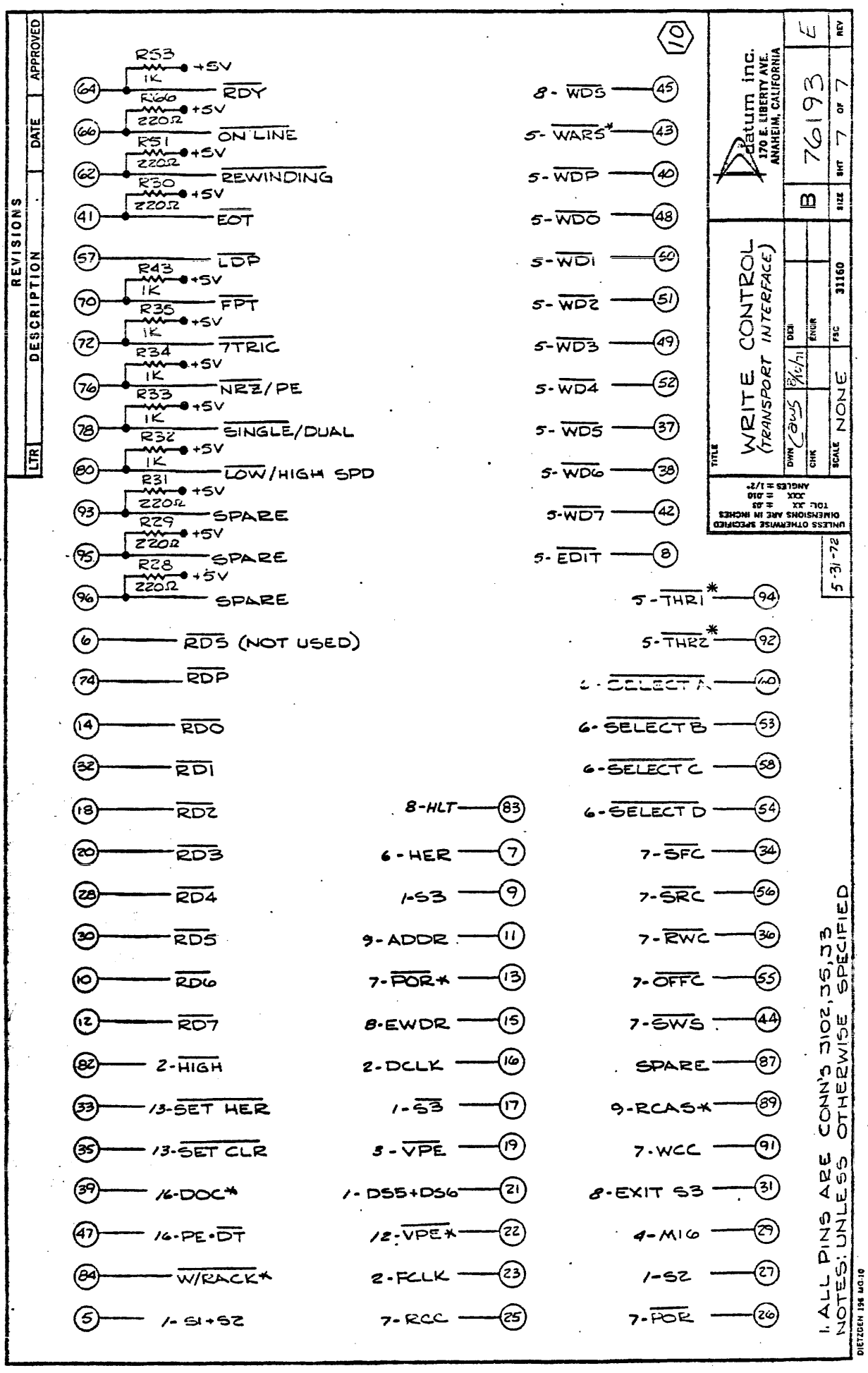
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ±.03 .XXX ±.010 ANGLES ±1/2°	TITLE: WRITE LOGIC (WRITE PHASE ENCODERS)			datum inc. 170 E. LIBERTY AVE. ANAHEIM, CALIFORNIA	
	DWN GWS 8/9/71	DES			
	CHK	ENGR			
5-31-72	SCALE NONE	FSC 31160		SIZE B	76192 B
				SHT 4 OF 4	REV


REVISIONS
LTR | DESCRIPTION | DATE | APPROVED
COMMAND REJECT LOGIC
HARD ERROR STATUS
TAPE UNIT SELECT
STATUS REGISTER
ID BURST STATUS
WRITE CONTROL
(REJECT, STATUS, SELECT)
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA
5-31-72
SCALE NONE
FSC 31160
B
76193
SHT 3 OF 7

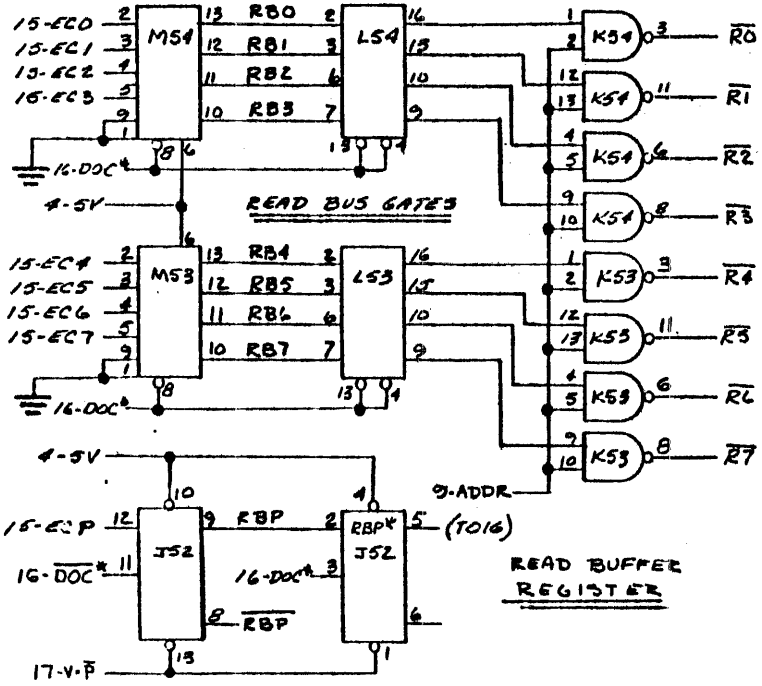

REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
9-SETWCC
9-SET WFM
9-SET GAP
9-SET RCC
9-SET REV
9-SET CLR
9-SET REW
6-VLD
WCC
WFM
GAP
RCC
BSR
CLR
RW
ADDR
WCC*
WCC+WFM
RCC*
BSR*
COMMAND REGISTER
9-SET REW
6-VLD
7-POR
10-LDP
6-WDG
REW
OFLC
10-ON LINE
OFLC
COMMAND REGISTER
7-WCC+WFM
7-GAP
9-ADDR
SWS
7-BSR
1-S1+S2+S3+S4
SRC
SFC
7-REW
7-OFLC
OFFC
TAPE TRANSPORT CONTROL
+5V
R52
1K
9-SET OFL
9-SET REW
E8
E9
(NEAR M27)
JUMPER FOR
"NO INT ON
REWIND"
6-VLD
1-DSO
1-S7
CBUSY
CBUST
P26
+20V
CR1
5G1930
R58
10K
R60
10K
C25
39μF
9-ADDR
9-EXT RESET
POR
7-POR
6-VLD
FOR*
FOR**
RESET LOGIC
7
5-31-72
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOL: .XX ±.03
.XXX ±.010
ANGLES ±1/2°
TITLE
WRITE CONTROL
(COMMAND REG XPORT CONTROL CRUS)
DWN CWS 8/4/71
DES
CHK
ENGR
SCALE NONE
FSC 31160
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA
B
76193
E
SIZE
SHT 4 OF 7
REV
DIETZGEN 196 MG-10

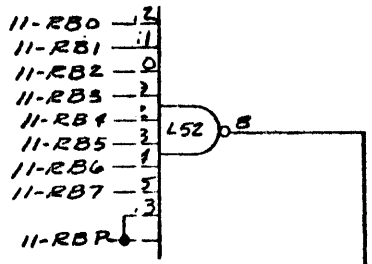

REVISIONS
LTR DESCRIPTION DATE APPROVED
WRITE PREAMBLE & FM SUBMODE
WRITE ID BURST & POST AMBLE SUBMODE
JUMPER FOR TEST SKEW CONTROL
WRITE ID BURST +5V
WRITE ALL ONE'S IN PRE-AMBLE
WRITE ALL ONE'S IN POST AMBLE
FCLK (FOR ID, PRE/POST AMBLE ALL ONES CHARACTER, FCLK ALL OTHER TIMES
DISABLE TRACKS 1,3,4 FOR FILE MARK
STATE 2 DISABLES ALL TRACKS BUT WDP FOR RE. IDENT BURST
IMS POST DELAY
ENABLE DELAY GATES
COUNTER RESET LOGIC
ENABLE WRITE DATA
ENABLE WRITE DATA REQUESTS
GATE WRITE STROBE CONTROL
SET SMI
SET SM2
EXITSS
IMSPD
IMSPD
RSTOP
CLKWB
CLKWB
P24-10 (TOS)
RST STOP
EWDR
EWDR
KSM2
JSM2
WDS
S3*
S26-8 (TOS)
FCLK*
EDATA
R24
S24
S22
S23
S25
S26
HLT
DSM2
GWDS
R64 1K
+5V
5VI
8
5-31-72
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ± .010 ANGLES ± 1/2°
TITLE
WRITE CONTROL
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA
DWN Cary 8/01/71
DES
CHK
ENGR
SCALE NONE
FSC 31160
B 76193 E
SIZE SHT 5 OF 7 REV
DIETZGEN 196 MG-10

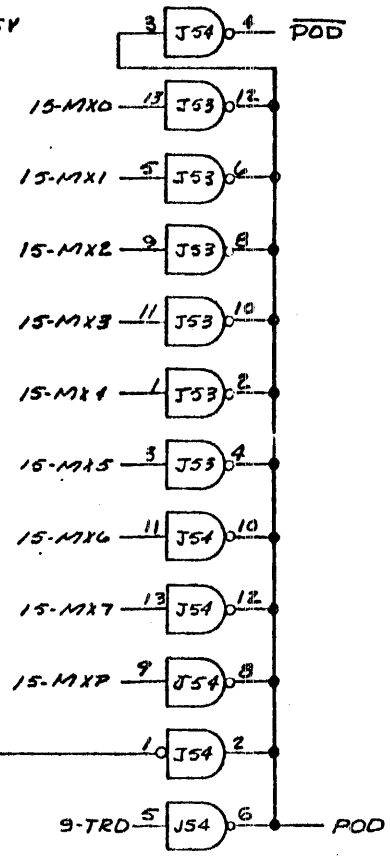

REVISIONS
LTR DESCRIPTION DATE APPROVED
Datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA
B 76193 E
SIZE SHT 6 OF 7 REV
TITLE WRITE CONTROL (COMPUTER ADAPTER INTERFACE)
DWN Cass 8/10/71 DES ENGR
CHK FSC 31160
SCALE NONE
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL .XX ± .03
.XXX ± .010
ANGLES ± 1/2°
5-31-72
10-NRZ
(NEAR 22)
NRZ E4
PE E5
E3
R79 1K +5V
ADDR
ADDRESS
ADDR
5-FORM SELECT
R78 680Ω
FADI 71
R10 +5V
E1 ZERO
E2 ONE
9-ADDR
STROBEC 5
STROBEC*
R46 +5V
1-53
4-STOP
THR1 6
THR2 8
EDIT 85
EDIT
R36 +5V
EXT RJCT 92
R2 +5V
EXT RESET 67
R54 +5V
HALT 72
R9 +5V
CD 29 (N/U)
HI DENSITY 77 (N/U)
GEN ODD PARITY 60
STOP SPACE 75
R57 +5V
SET REV 90
R4 +5V
SET WCC 32
R38 +5V
TRD 69
+5
SET WFM 55
R44 +5V
SET GAP 57
R45 +5V
SET FSR 89
R3 +5V
SET RCC 58
R62 +5V
SETCLR 64
R11 +5V
SETREW 68
R65 +5V
SETOFL 61
R13 +5V
SPARE 14
SPARE 12
SPARE 10
B0 37
R39 +5V
B1 62
R12 +5V
B2 39
R41 +5V
B3 42
R42 +5V
B4 45
R17 +5V
B5 52
R14 +5V
B6 40
R16 +5V
B7 49
R15 +5V
W/RACK 7
R73 +5V
5-DBY 65
R37 +5V
3-CBUSY* 94
R67 +5V
R7 +5V 78 -RCAS*
6-RJCT 76
R8 +5V
16-POST 79
16-CKWD
R1 +5V
CK WD CNT
16-DATA FLAG 82
R6 +5V
7-WCC 31
R56 +5V
7-RCC 38
R55 +5V
2-K1 9-ADDR
R71 +5V 69 WRMSB
16-TMER 87
1K 281 +5
6-PARITYER 93
R68 +5V
5-RDY
3-FM 70
R40 +5V
95
9-SET WCC
SET RJCT
6-RWDG 9
R59 +5V
10-FPI 45
9-SET WFM
10-LDP 47
9-SET GAP
SET RJCT
6-EOTS 59
R72 +5V
6-REJECT 80
R70 +5V
SET CLR
5-9TRK 73
REV+CLR
9-SET REV
16-RP 19
R23 +5V
11-RO 15
R25 +5V
11-R1 26
R20 +5V
11-R2 17
R24 +5V
11-R3 25
R21 +5V
11-R4 11
R27 +5V
11-R5 30
R18 +5V
11-R6 13
R26 +5V
11-R7 28
R19 +5V
S1 91
R69 +5V
S1
S2 84
R5 +5V
S2
9-A32-4
RCAS*
10-LOW/HIGH 20
16-RSTROBE 21
R22 +5V
6-IDENTS 41
R50 +5V
2-CLR 34
R47 +5V
2-WRP 88
R48 +5V
10-NRZ/PE 24
10-SINGLE/DUAL 22
W/RACK*
W/RACK*
6-CERS 40
R49 +5V
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 220Ω
2. ALL PINS ARE CONN'S 31,01,32,34,36
EIETZGEN 196 MO 10

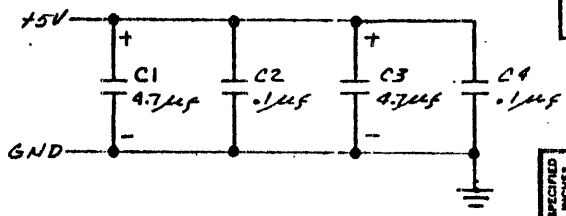

REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
10
RS3 1K +5V
64 RDY
R66 220Ω +5V
66 ON LINE
RS1 220Ω +5V
62 REWINDING
R30 220Ω +5V
41 EOT
57 LDP
R43 1K +5V
70 FPT
R35 1K +5V
72 TTRIC
R34 1K +5V
76 NRZ/PE
R33 1K +5V
78 SINGLE/DUAL
R32 1K +5V
80 LOW/HIGH SPD
R31 220Ω +5V
93 SPARE
R29 220Ω +5V
95 SPARE
R28 220Ω +5V
96 SPARE
6 RDS (NOT USED)
74 RDP
14 RDO
32 RD1
18 RD2
20 RD3
28 RD4
30 RD5
10 RD6
12 RD7
82 2-HIGH
33 13-SET HER
35 13-SET CLR
39 16-DOC*
47 16-PE·DT
84 W/RACK*
5 1-S1+S2
8 - WDS 45
5 - WARS* 43
5 - WDP 40
5 - WDO 48
5 - WD1 50
5 - WD2 51
5 - WD3 49
5 - WD4 52
5 - WD5 37
5 - WD6 38
5 - WD7 42
5 - EDIT 8
8-HLT 83
6 - HER 7
1-S3 9
9-ADDR 11
7-POR* 13
8-EWDR 15
2-DCLK 16
1-S3 17
3 - VPE 19
1 - DS5+DS6 21
12-VPE* 22
2-FCLK 23
7-RCC 25
5 - THR1* 94
5 - THR2* 92
6 - SELECT A 100
6 - SELECT B 53
6 - SELECT C 58
6 - SELECT D 54
7 - SFC 34
7 - SRC 56
7 - RWC 36
7 - OFFC 55
7 - SWS 44
SPARE 87
9 - RCAS* 89
7 - WCC 91
8 - EXIT S3 31
4 - M16 29
1 - S2 27
7 - POR 26
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA
E
B
76193
SHT 7 OF 7
REV
SIZE
WRITE CONTROL
(TRANSPORT INTERFACE)
TITLE
DWN Lewis
CHK
ENGR
FSC 31160
SCALE NONE
5-31-72
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOL .XX ± .03
.XXX ± .010
ANGLES ± 1/2°
1. ALL PINS ARE CONN'S 3102, 35, 33
NOTES: UNLESS OTHERWISE SPECIFIED
DIETZGEN 196 MO.10

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED









H52		K52		M52	
PIN	TERM	PIN	TERM	PIN	TERM
1	CLOCK	1	DOC*	1	N.C.
2	END	2	DOC*	2	9-TRD
3	POD	3	R2	3	EC7
4	MX3	4	R0	4	EC6
5	MX2	5	R6	5	EC5
6	MXP	6	R4	6	EC4
7	VPE*	7	GND	7	GND
8	MX0	8	R5	8	J52-5
9	MX1	9	17-V-P	9	N.C.
10	MX7	10	R7	10	EC3
11	MX6	11	R1	11	EC2
12	MX5	12	R3	12	EC1
13	MX4	13	ADDR	13	EC0
14	ECP	14	+5V	14	+5V

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL .XX = .03
.XXX = .010
ANGLES = 1/2°

TITLE
READ LOGIC
(READ REG'S & POSTAMBLE DETECT)

DWN R.BUTO	7/14/71	DES	
CHK		ENGR	
SCALE —		FSC 31160	

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

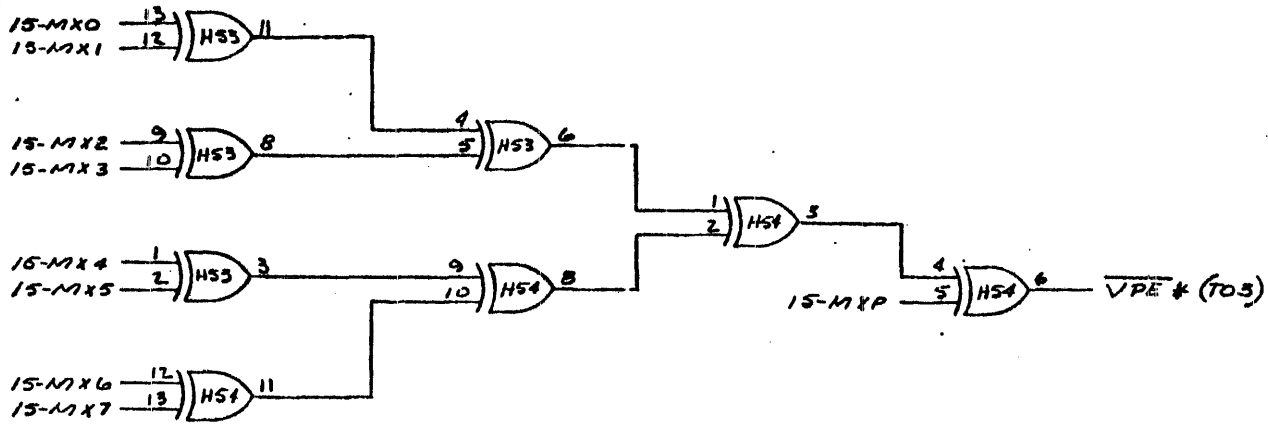
SIZE	SHT	REV
B	2 OF 3	

76181

11

DIETZGEN 196 MG-10

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



READ ODD PARITY CHECK

12

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL .XX ± .03
.XXX ± .010
ANGLES ± 1/2°

TITLE: READ LOGIC (PARITY CHECK)

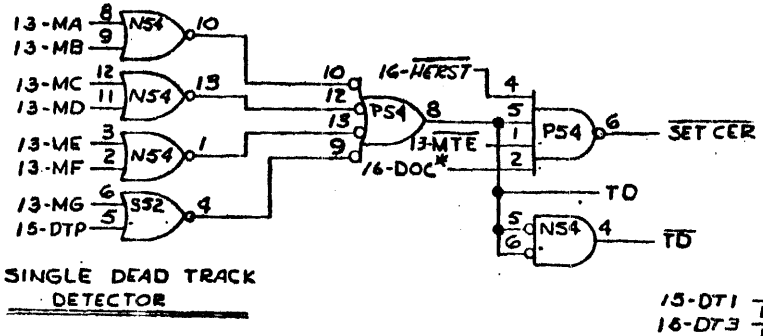
DWN PIZUTO	6/16/71	DES	
CHK		ENGR	
SCALE —		FSC 31160	

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

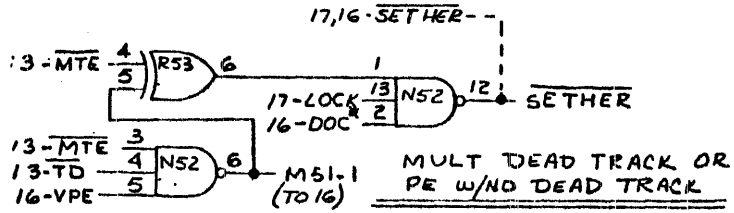
B | 76181 | SHT 3 OF 3 | REV

DIETZGEN 196 MG-10

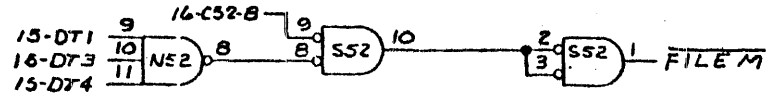
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



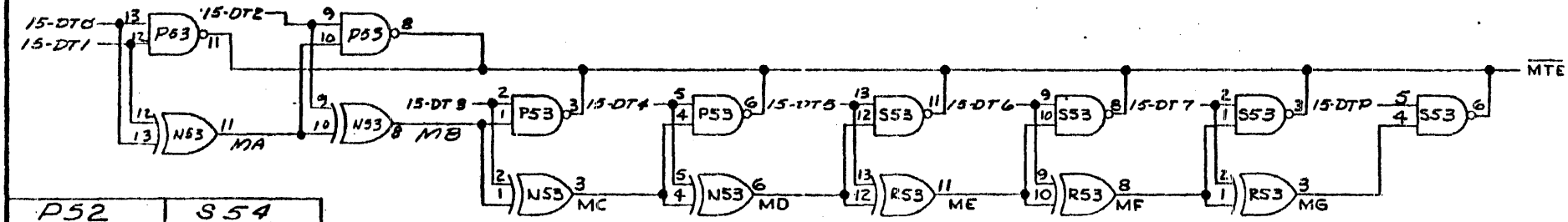
SINGLE DEAD TRACK DETECTOR



MULT DEAD TRACK OR PE W/NO DEAD TRACK

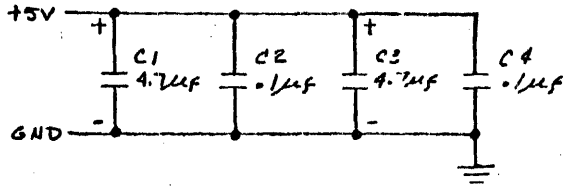


FILE MARIC DETECT



MULTIPLE DEAD TRACK DETECTOR

P52		S54	
PIN	TERM	PIN	TERM
1	DTP	1	FILEM
2	DT6	2	N.C.
3	DT7	3	N.C.
4	DT5	4	N.C.
5	VPE	5	C52-B
6	MS1-1	6	TD
7	GND	7	GND
8	DT1	8	SETCER
9	DT2	9	TD
10	DT3	10	MS1-B
11	DT4	11	SETHER
12	DT0	12	LOCK
13	DOC*	13	MTE
14	+5V	14	+5V



13

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ±.03 .XXX ±.010 ANGLES ±1/2°

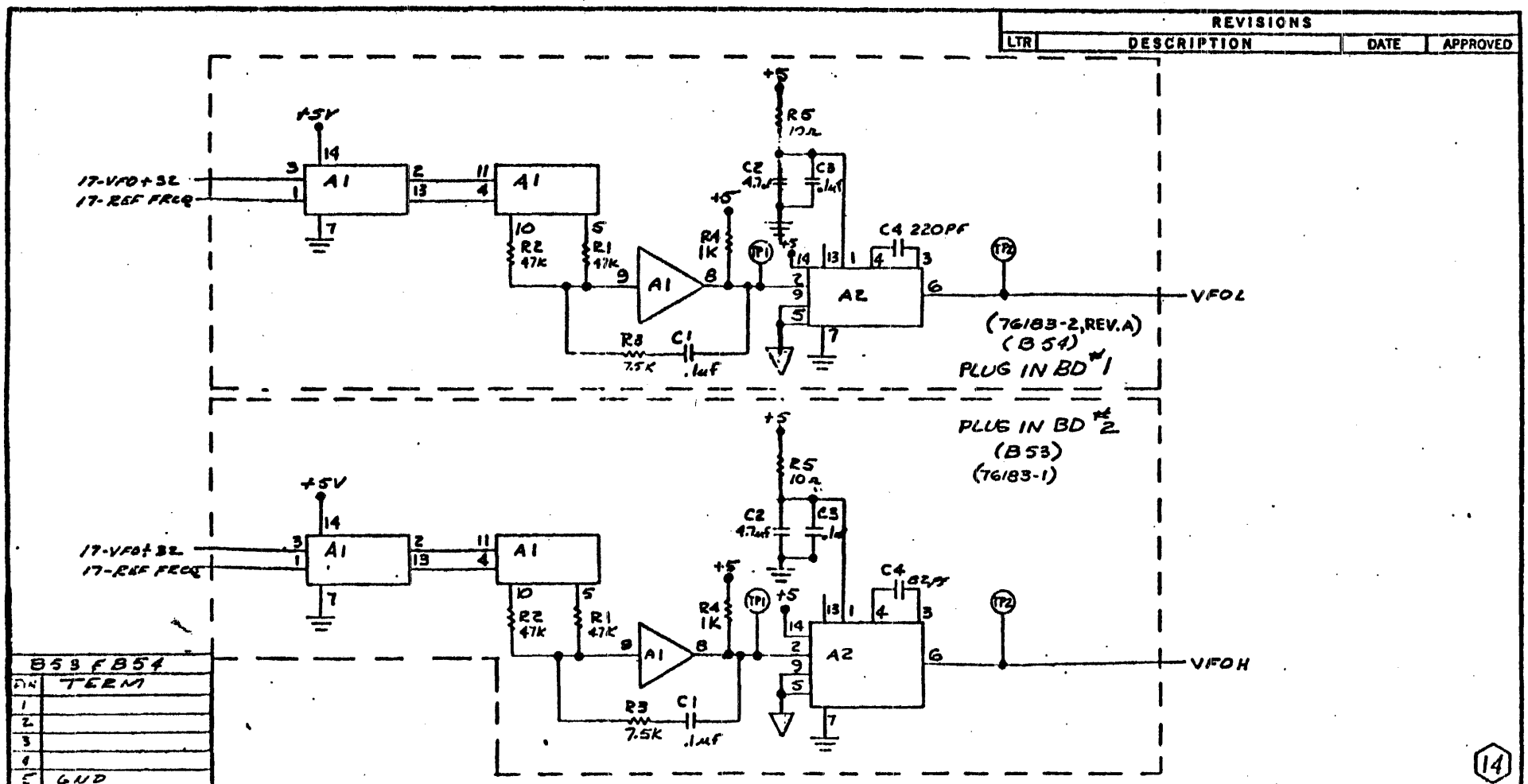
TITLE: DEAD TRACK DETECTOR

DWN Rizuto 6/16/71 | DES | CHK | ENGR | SCALE —— | FSC 31160

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

B | 76180 | SIZE | SHT 2 OF 2 | REV

DIETZGEN 196 MQ-10



B53 & B54	
PIN	TERM
1	
2	
3	
4	
5	GND
6	VFOH & VFOL
7	GND
8	GND
9	
10	
11	
12	VFO ÷ 32
13	REF FREQ
14	+5V

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ±.03 .XXX ±.010 ANGLES ±1/2°

TITLE: VOLTAGE CONTROL OSC.

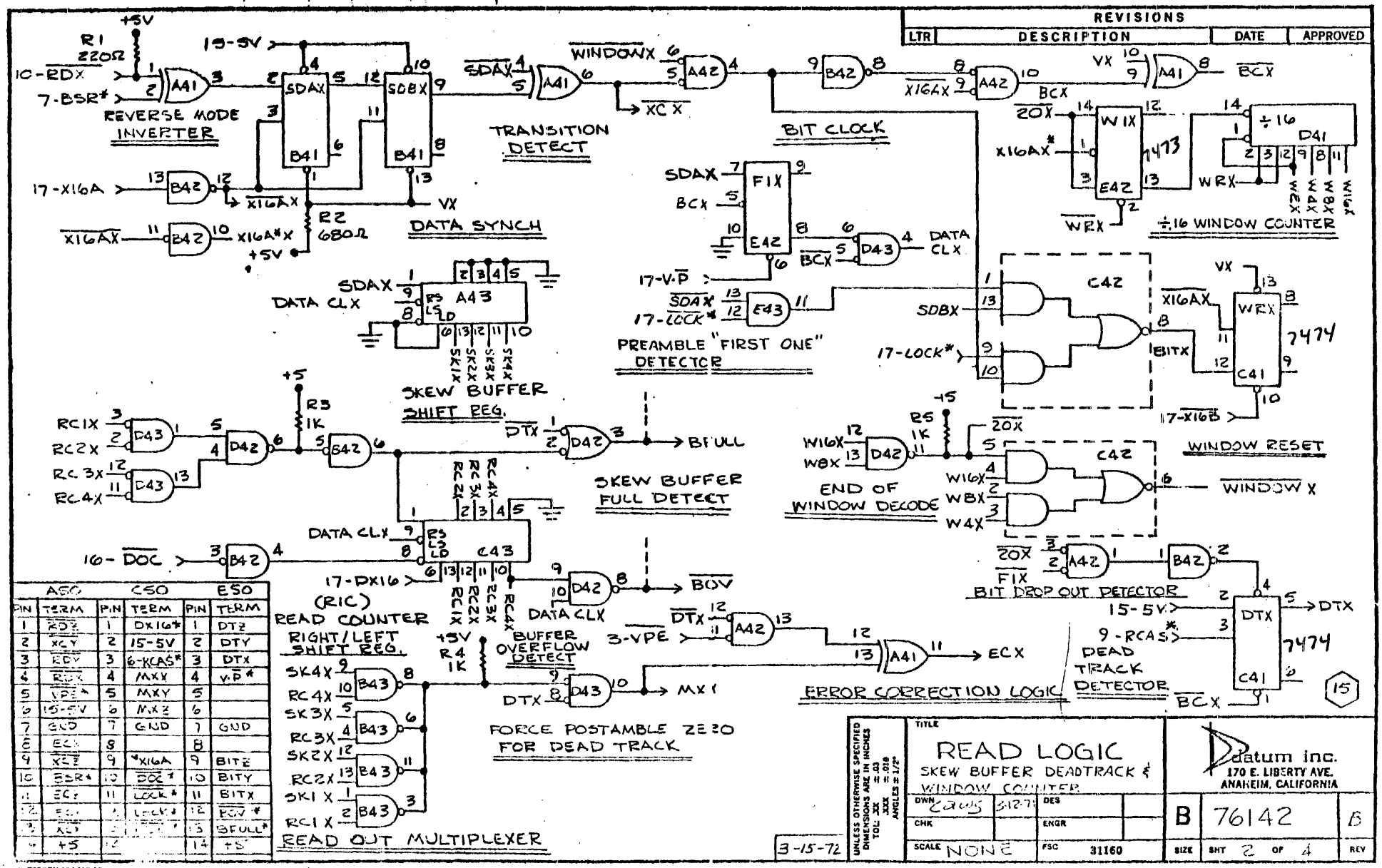
DWN RIZUTO 6/12/81 | DES | CHK | ENGR | SCALE | FSC 31160

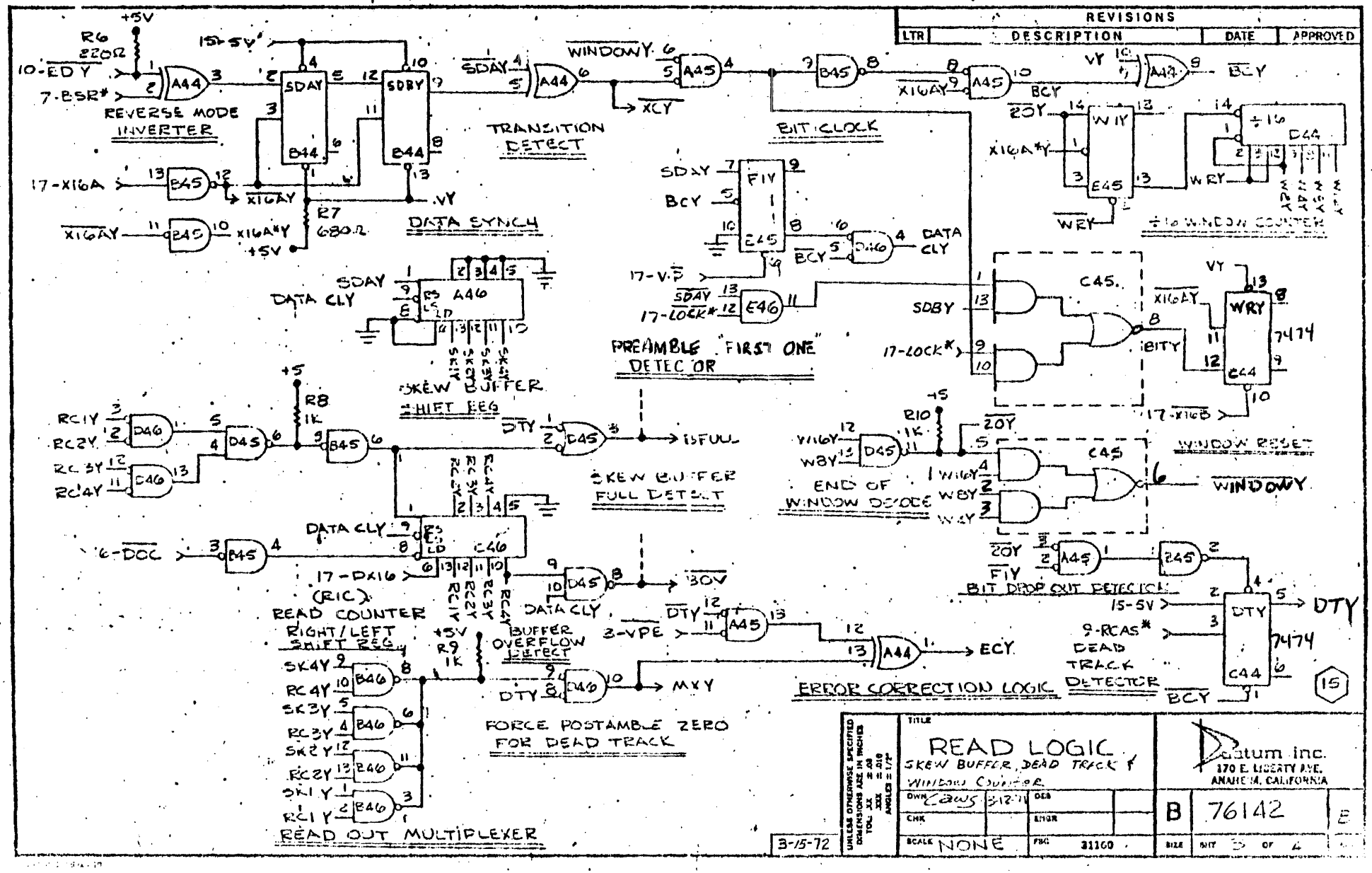
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

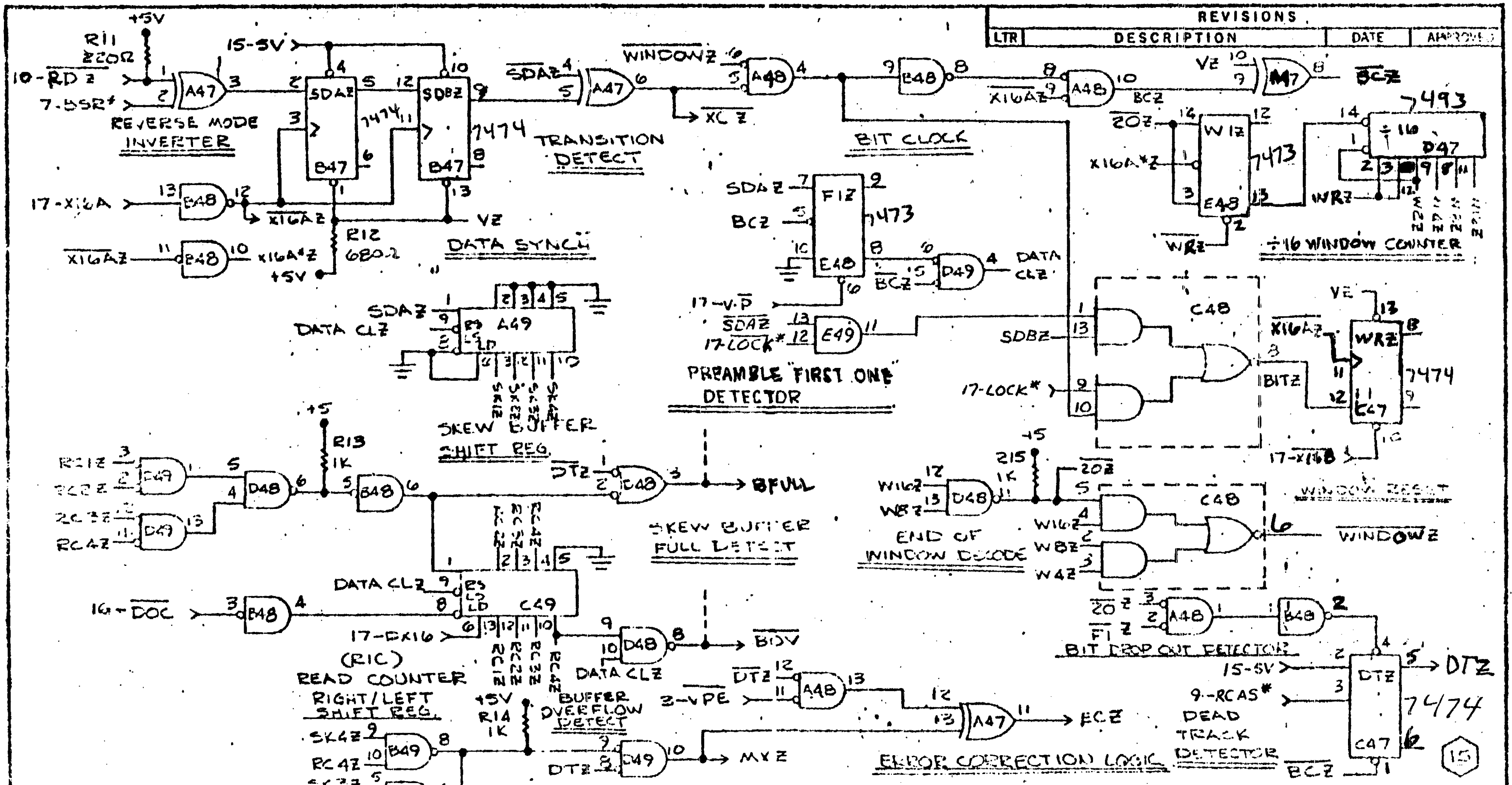
B | 76183 | SIZE | SHT 2 OF 2 | REV

14

DIETZGEN 196 MG 10


REVISIONS
LTR | DESCRIPTION | DATE | APPROVED
REVERSE MODE INVERTER
TRANSITION DETECT
BIT CLOCK
DATA SYNCH
÷16 WINDOW COUNTER
SKEW BUFFER SHIFT REG.
PREAMBLE "FIRST ONE" DETECTOR
SKEW BUFFER FULL DETECT
END OF WINDOW DECODE
WINDOW RESET
BIT DROP OUT DETECTOR
(RIC) READ COUNTER
RIGHT/LEFT SHIFT REG.
BUFFER OVERFLOW DETECT
FORCE POSTAMBLE ZERO FOR DEAD TRACK
DEAD TRACK DETECTOR
ERROR CORRECTION LOGIC
READ OUT MULTIPLEXER
ASO
CSO
ESO
READ LOGIC
SKEW BUFFER DEADTRACK & WINDOW COUNTER
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA
76142
3-15-72


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
+5V
R6
220Ω
10-EDY
7-BSR*
REVERSE MODE INVERTER
A44
SDAY
SDBY
B44
TRANSITION DETECT
WINDOWY
A45
XCY
B45
BIT CLOCK
X16AY
BCY
VY
A47
17-X16A
X16AY
R7
680Ω
DATA SYNCH
SDAY
DATA CLY
A46
SKEW BUFFER SHIFT REG
F1Y
E45
17-V.P
E46
17-LOCK*
PREAMBLE "FIRST ONE" DETECTOR
C45.
SDBY
BITY
WRY
C44
7474
20Y
W1Y
÷16 D44
÷16 WINDOW COUNTER
WINDOW RESET
R8
1K
RC1Y
RC2Y
RC3Y
RC4Y
D46
D45
SKEW BUFFER FULL DETECT
15FULL
R10
W16Y
W8Y
W4Y
W2Y
W1Y
END OF WINDOW DECODE
6-DOC
17-DX16
(RIC) READ COUNTER RIGHT/LEFT SHIFT REG
30V
R9
1K
BUFFER OVERFLOW DETECT
DTY
3-VPE
ECY
A44
ERROR CORRECTION LOGIC
FIY
BIT DROP OUT DETECTION
15-5V
9-RCAS*
DEAD TRACK DETECTOR
C44
7474
MXY
FORCE POSTAMBLE ZERO FOR DEAD TRACK
SK4Y
SK3Y
SK2Y
SK1Y
B46
READ OUT MULTIPLEXER
15
3-15-72
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL .XX ± .03
.XXX ± .010
ANGLES ± 1/2°
TITLE
READ LOGIC
SKEW BUFFER, DEAD TRACK & WINDOW COUNTER
DWN
CHK
ENGR
DES
SCALE NONE
FSC 31160
Datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA
B
76142
SIZE
SHT 5 OF 6



READ LOGIC

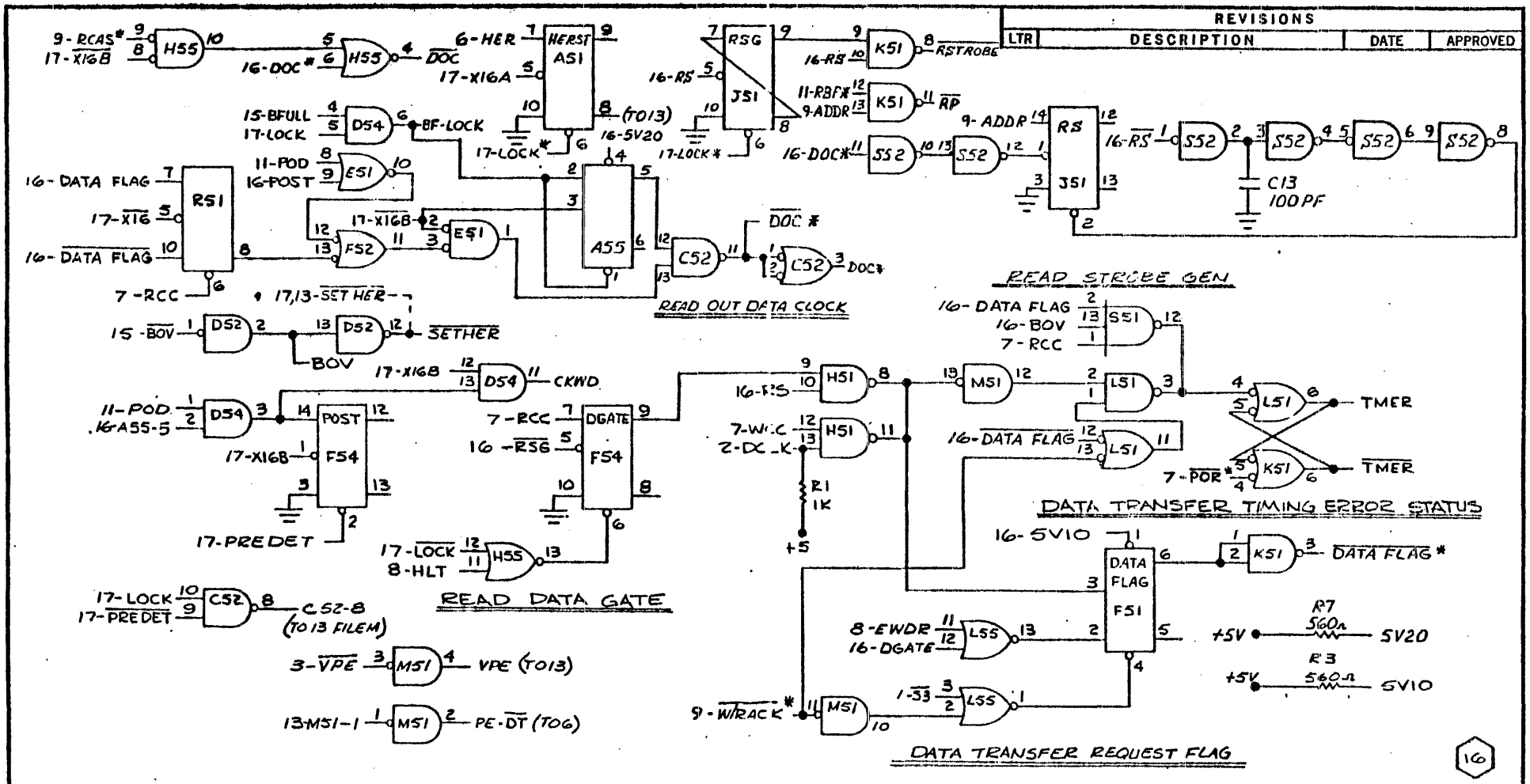
SKEW BUFFER, DEAD TRACK & WINDOW COUNTER

Datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX = .03 .XXX = .010 ANGLES = 1/2°

DWN C. Lewis	3-12-71	CKD	
CHK		ENGR	
SCALE NONE		PROJ 31170	

SIZE	DWG NO.	REV
B	76142	B
	SHT 4 OF 4	



NOTE : UNLESS OTHERWISE SPECIFIED

5-31-72

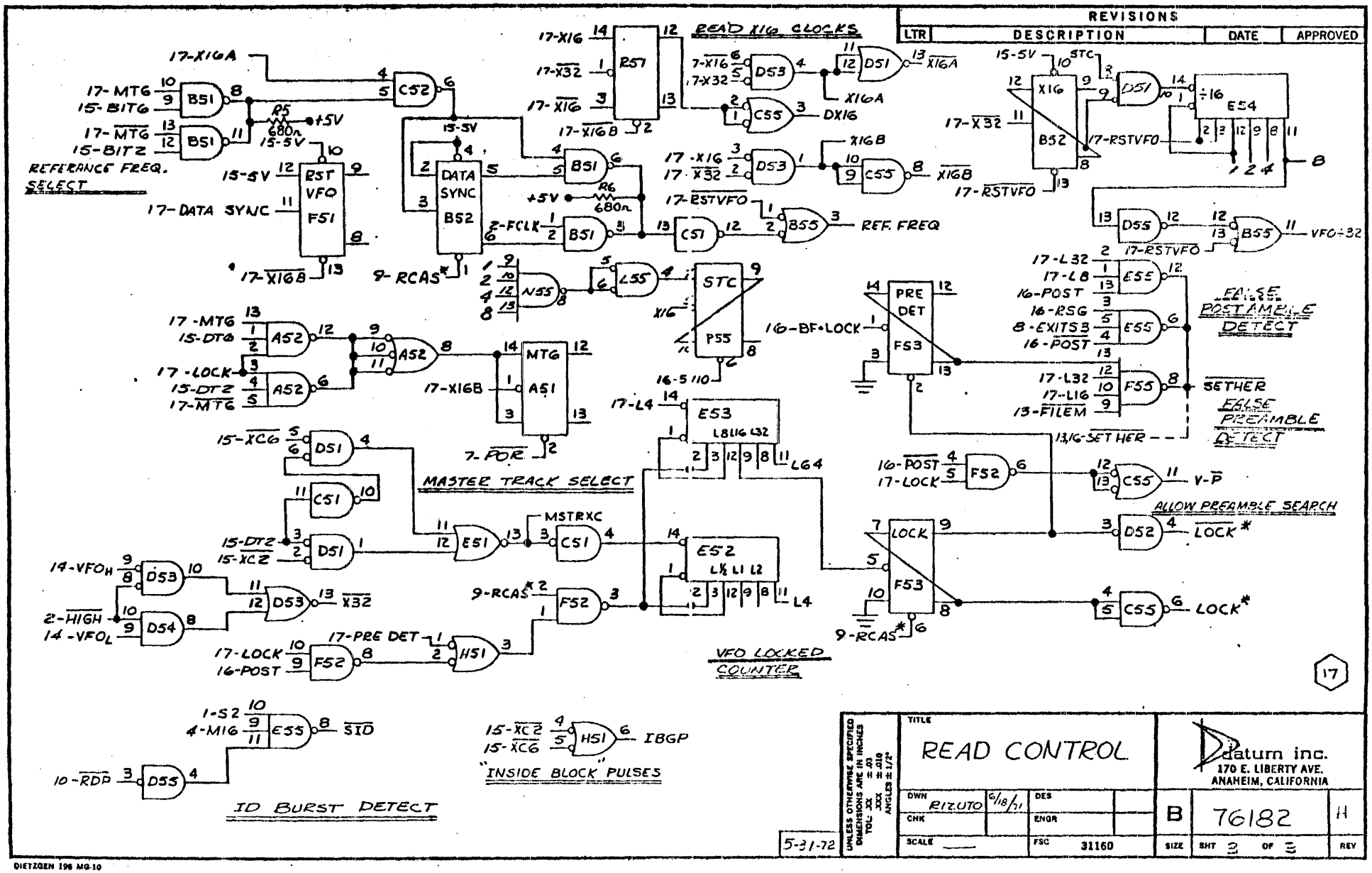
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

TITLE: READ CONTROL

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN RIZUTO 6/17/71	DES	B	76182 H
CHK	ENGR		
SCALE —	FSC 31160	SIZE	SHT 2 OF 3 REV

DIETZGEN 196 MQ-10



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

TITLE: READ CONTROL

DWN RIZUTO 6/18/71 DES
CHK ENGR
SCALE —— FSC 31160

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

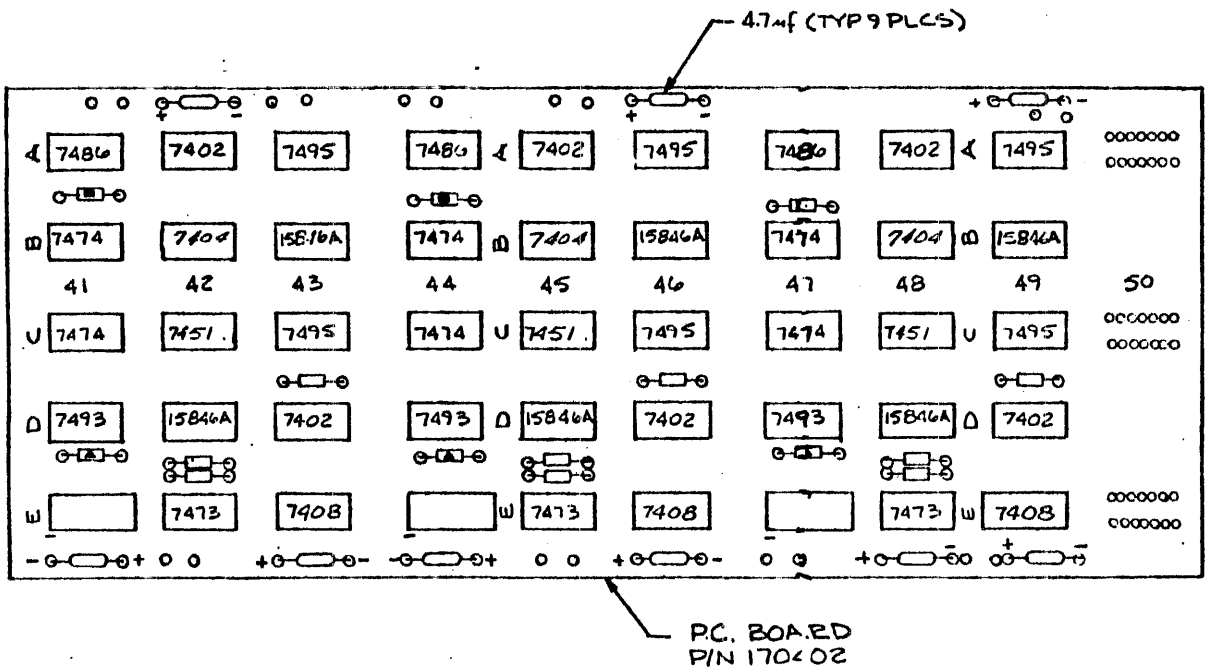
SIZE B | 76182 | REV H

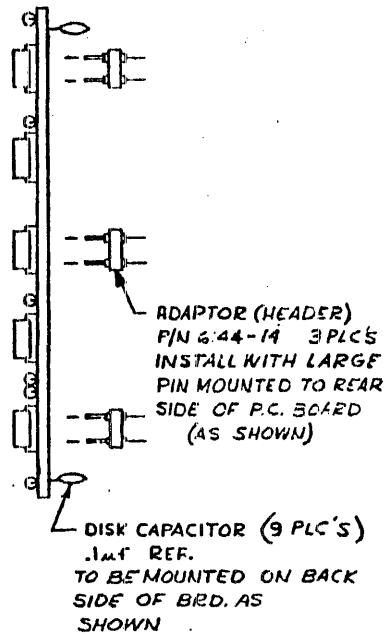
SHT 3 OF 3

5-31-72

DIETZGEN 196 MG-10

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED





3. ■ DENOTES 220Ω RESISTOR 1/4 W 5%
2. ▲ DENOTES 680Ω RESISTOR 1/4W 5%
1. ALL RESISTORS ARE 1K, 1/4W 5%

NOTES: UNLESS OTHERWISE SPECIFIED

3-15-72

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL .XX ± .03
.XXX ± .010
ANGLES ± 1/2°

TITLE: READ LOGIC

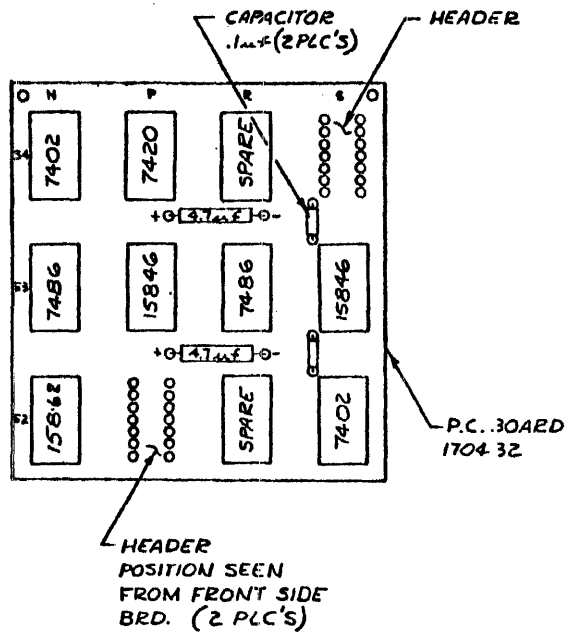
DWN Laws 3-13-72 | DES
CHK | ENGR
SCALE FULL | FSC 31160

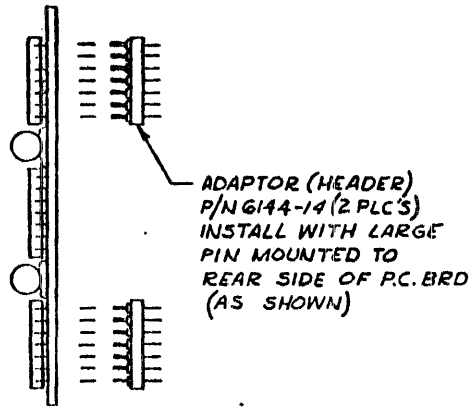
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

B | 76142 | B
SIZE | SHT 1 OF 4 | REV

DIETZGEN 196 MQ-10

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED





NOTES.

1. THE EQUIVALENTS OF 15862 IS DM962, AND 15846 IS DM946.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: .XX ± .03
.XXX ± .010
ANGLES ± 1/2°

TITLE: DEAD TRACK DETECTOR

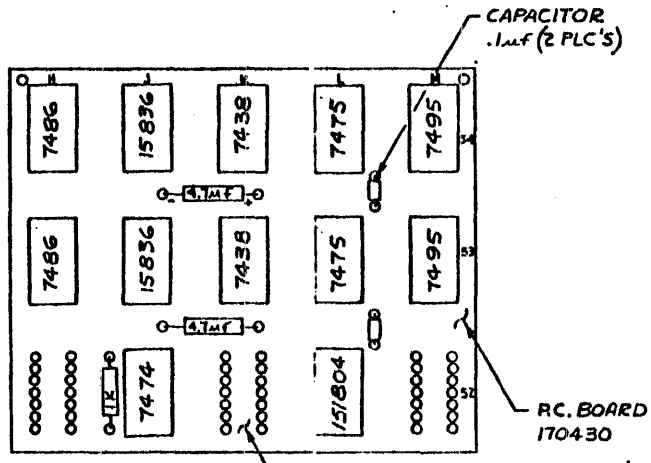
DWN RIZUTO 7/9/71 | DES [illegible] 7/9/71 | CHK [illegible] | ENGR | SCALE FULL | FSC 31160

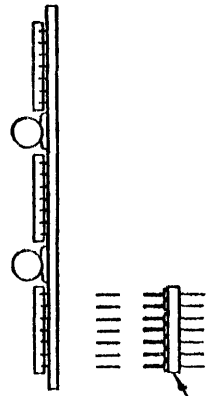
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

B | 76180 | SIZE | SHT 1 OF 2 | REV

DIETZGEN 195 MG-10

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED





NOTES:

1. THE EQUIVALENT OF 15836 IS DM936N.

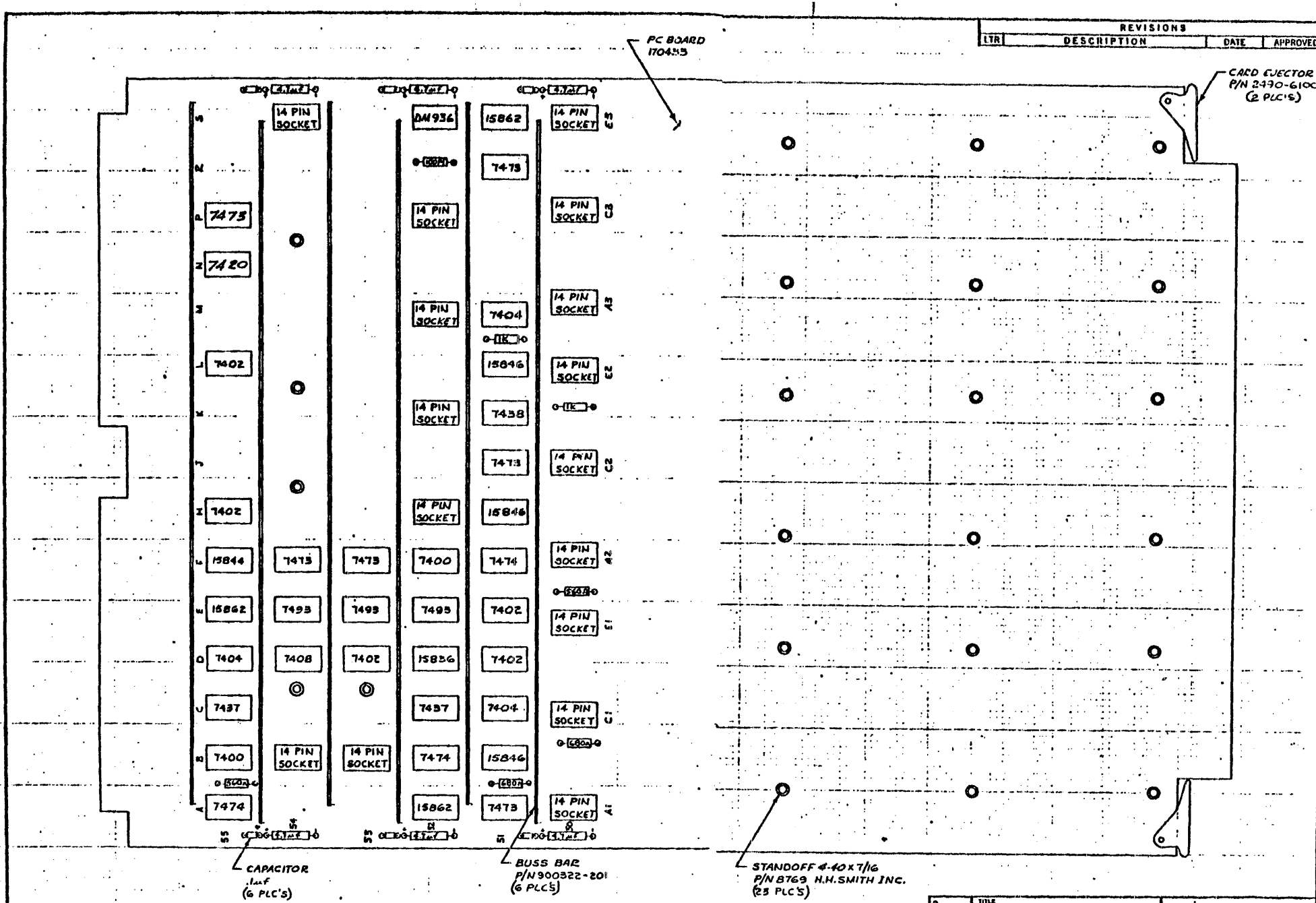
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: .XX ± .03, .XXX ± .010, ANGLES ± 1/2°

TITLE: READ LOGIC

DWN RIZUTO	7/19/71	DES M. FADDEN	7/19/71		
CHK	7/19/71	ENGR			
SCALE FULL		FSC 31160		SIZE B	76181
				SHT 1 OF 3	REV

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DIETZGEN 196 MG-10



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

1. THE EQUIVALENT OF: 15836 IS DM936N, 15844 IS DM944N, 15846 IS DM946N, AND 15862 IS DM962N.

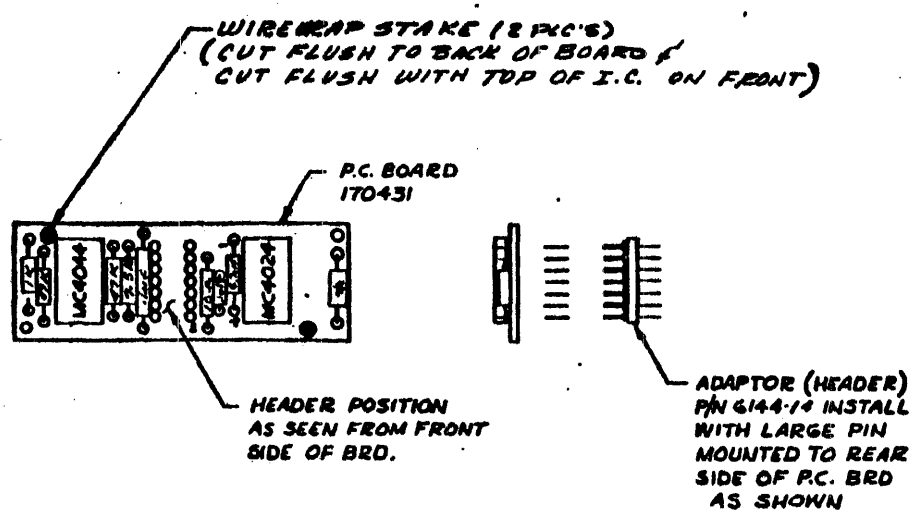
NOTES: UNLESS OTHERWISE SPECIFIED

TITLE	READ CONTROL		
DWN	BIZUR 5/11/	DES	
CHK		ENGR	
SCALE	——	FSC 31160	
		SIZE	76182
		SHT 1 OF 3	REV

datum inc. 170 E. LIBERTY AVE. ANAHEIM, CALIFORNIA

5-31-72

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



DASH NO.	TAPE SPEED	C4 #
-1	37.5 TO 75	82 pf
-2	12.5 TO 25	220 pf

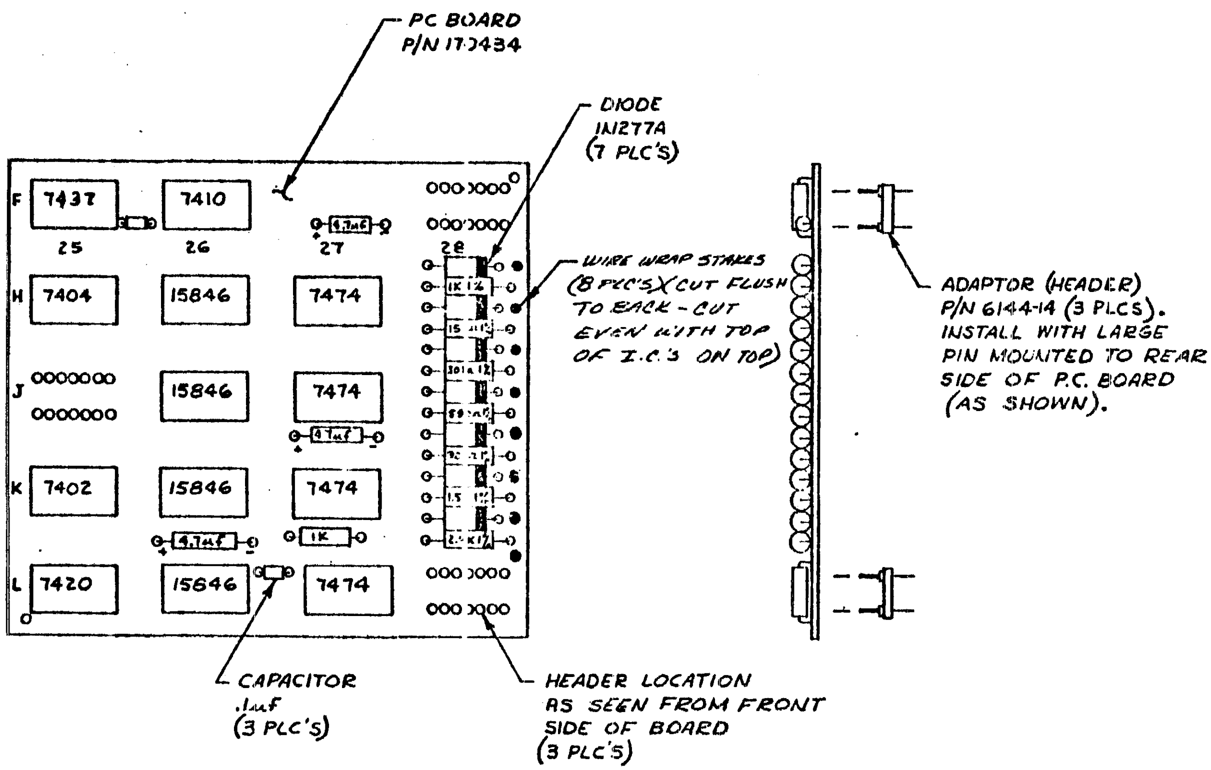
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL .XX ± .03
.XXX ± .010
ANGLES ± 1/2°

TITLE
VOLTAGE CONTROL OSC.

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN RIZUTO		DES		B	76183
CHK		ENGR			
SCALE FULL		FSC 31160		SIZE	SHT 1 OF 2 REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



1. DM946N IS EQUIVALENT TO 15846.

NOTES: [illegible]LESS OTHERWISE SPECIFIED

4-18-72

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

TITLE: STATE COUNTER

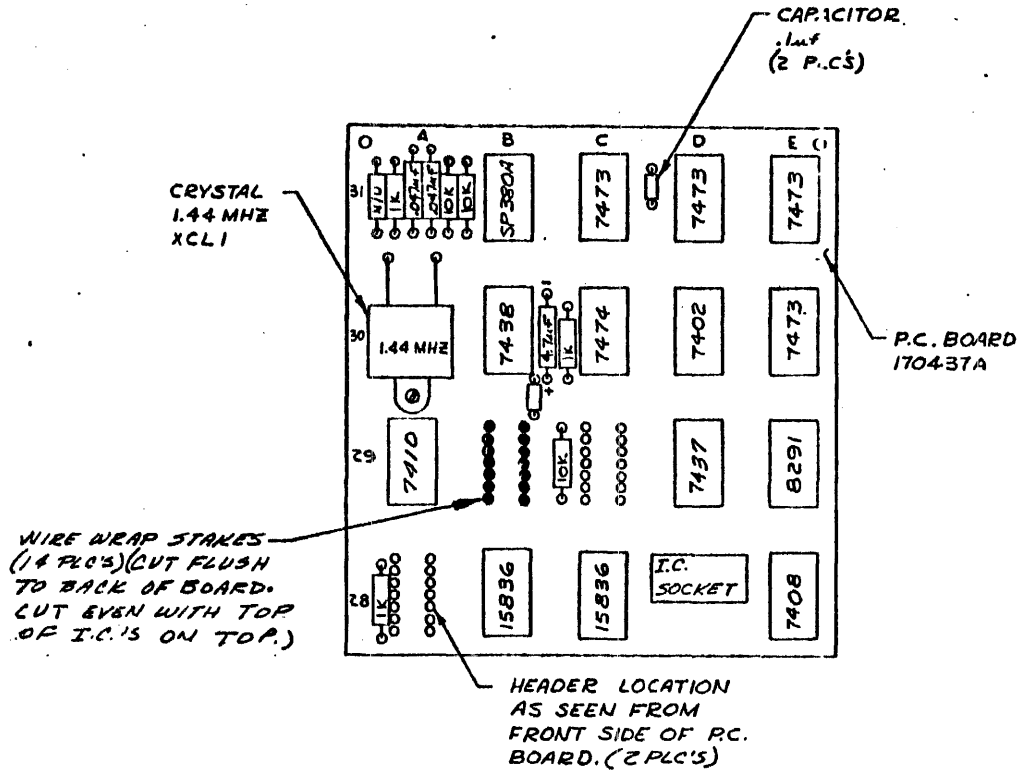
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

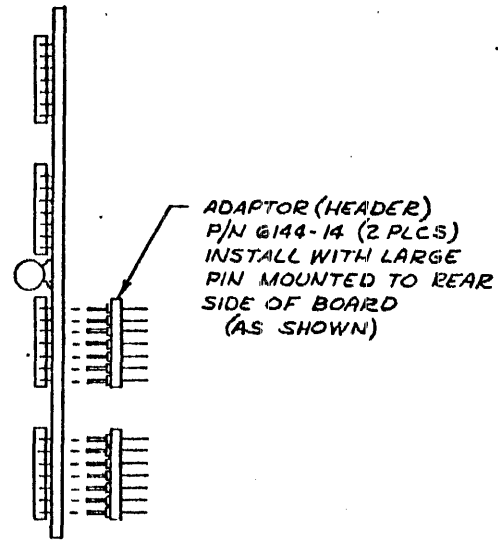
DWN RIZUTO	7/21/71	DES [illegible]	[illegible]
CHK [illegible]	[illegible]	ENGR	
SCALE FULL		FSC 31160	

SIZE	DWG NO.		REV
B	76190		
	SHT 1	OF 2	

DIETZGEN 196 MG-10

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED





1. THE EQUIVALENTS OF: 15836 IS DM936N AND 15862 IS DM962N.

NOTES: UNLESS OTHERWISE SPECIFIED

3-15-72

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ± .010 .XXX ± .005 ANGLES ± 1/2°

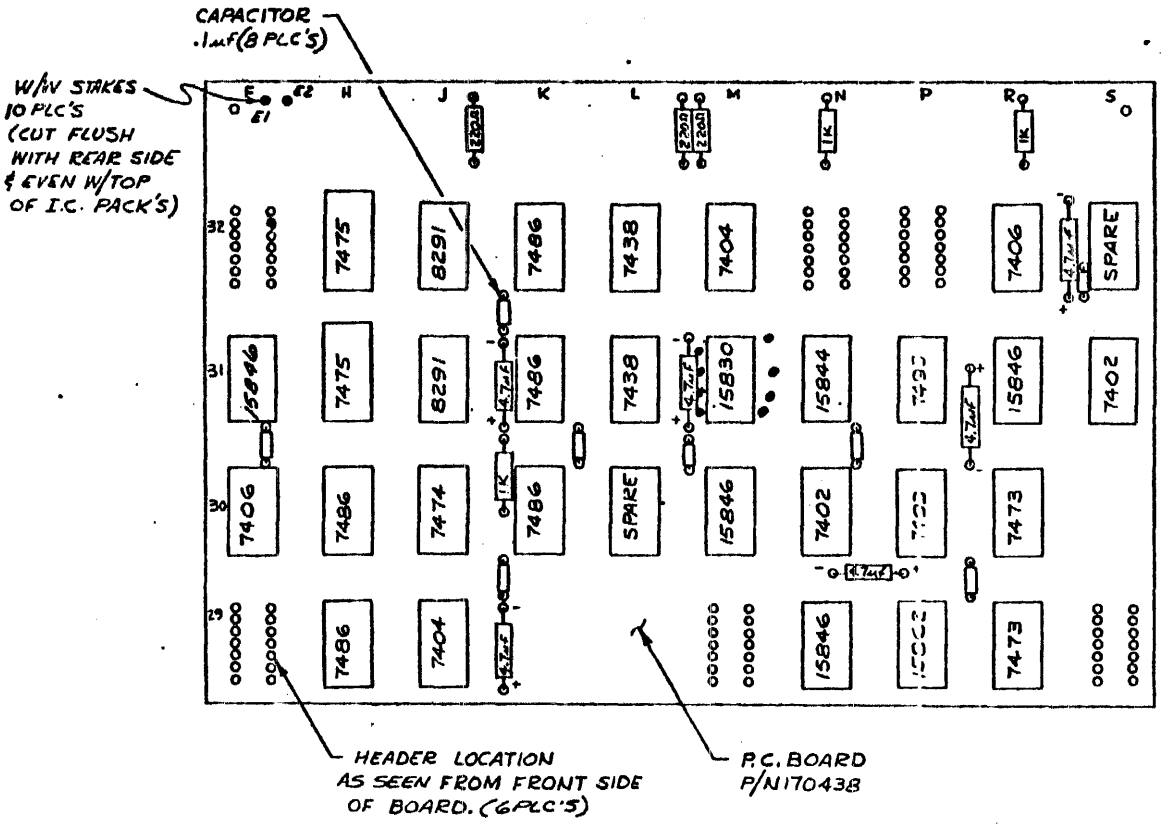
TITLE: OSCILLATOR BOARD

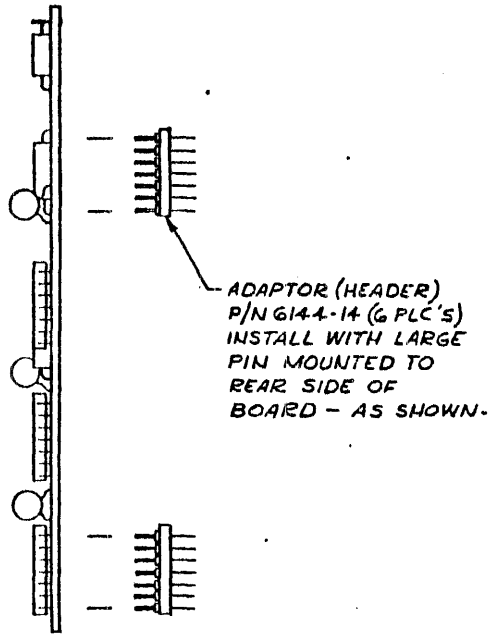
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN S. RIZUTO	7/27/71	DES [illegible]	7/27/71	B	76191 A
CHK [illegible]	7/27/71	ENGR			
SCALE FULL		FSC 31160		SIZE	SHT 1 OF 3 REV

DIETZGEN 196 MG 10

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED





1. THE EQUIVALENTS OF: 15844 IS DM944N, 15846 IS DM946N AND 15862 IS DM962N.

NOTES: UNLESS OTHERWISE SPECIFIED

5-31-72

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: XX ±.03, XXX ±.010, ANGLES ±1/2°

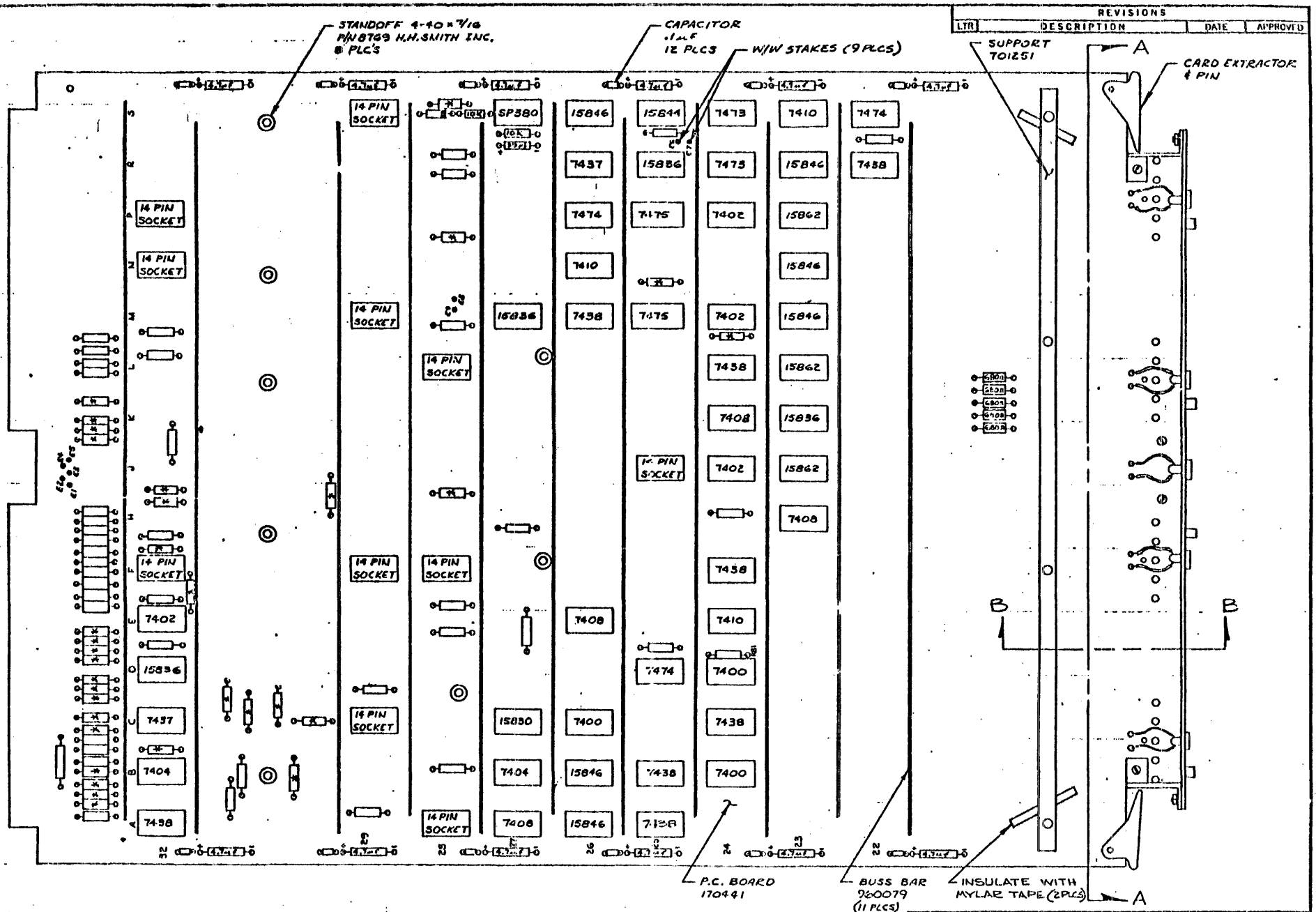
TITLE: WRITE LOGIC

DWN	CHK	SCALE	DES	ENGR	FSC
RIZUTO 7/28/71		FULL			31160

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

SIZE		SHT	OF	REV
B	76192	1	4	B

DIETZGEN 196 MG 10



4. THE EQUIVALENTS OF: 1583615 DM936N, 15844 IS DM944N, 15846N IS DM946N, AND 15862 IS DM926N.
3. * DENOTES RESISTOR 220Ω, 1/4W, 5%
2. DIODE IS 5G1930
1. RESISTORS ARE 1K 1/4W 5%

NOTES: UNLESS OTHERWISE SPECIFIED

LTR	DESCRIPTION	DATE	APPROVED
REVISIONS			

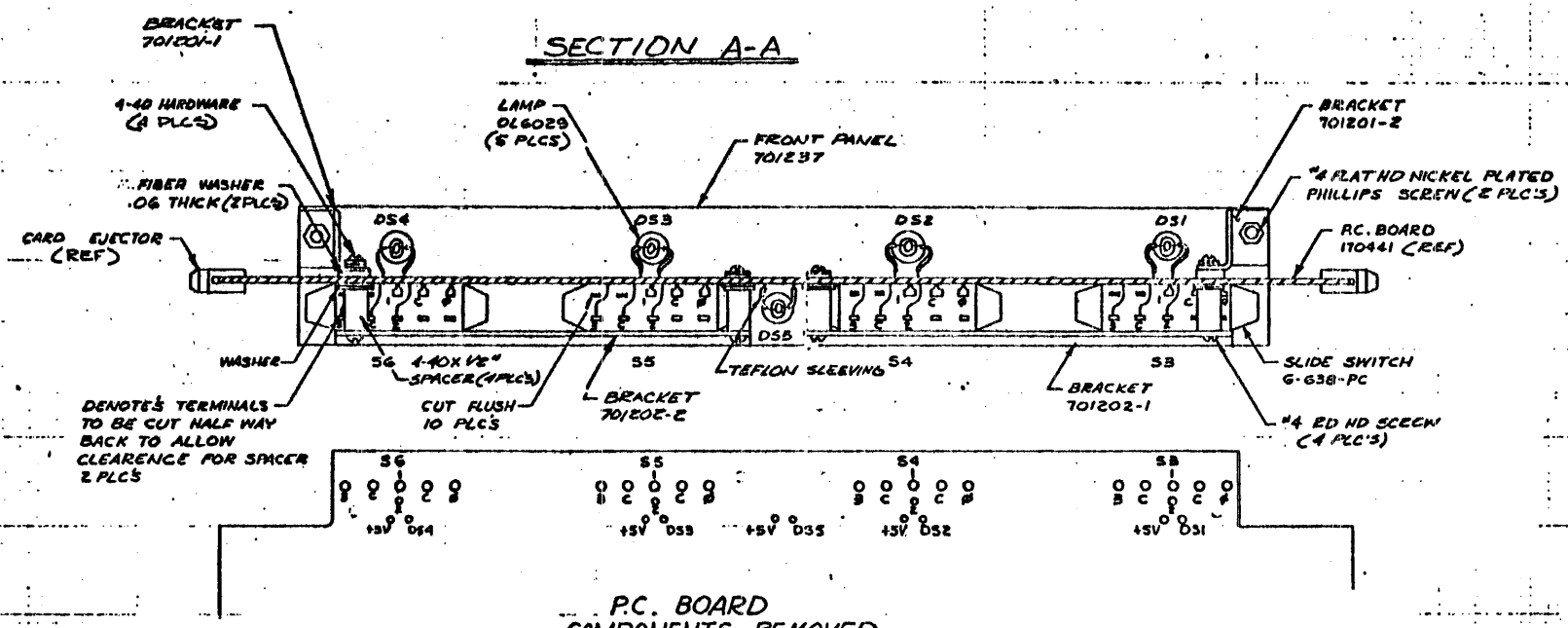
TITLE	WRITE CONTROL		
DRN	RIDTO	DES	
CHK		ENGR	
SCALE		FSC	31160
SIZE	C	76193	REV E
SHT	1 OF 2		

Datum Inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

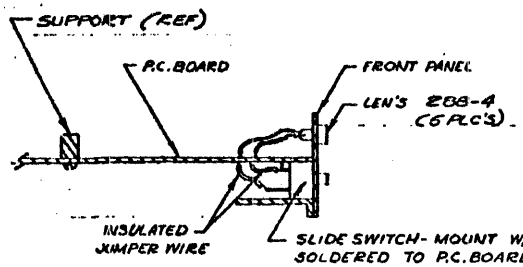
5-31-72

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

SECTION A-A



P.C. BOARD COMPONENTS REMOVED FOR CLARITY



SECTION B-B

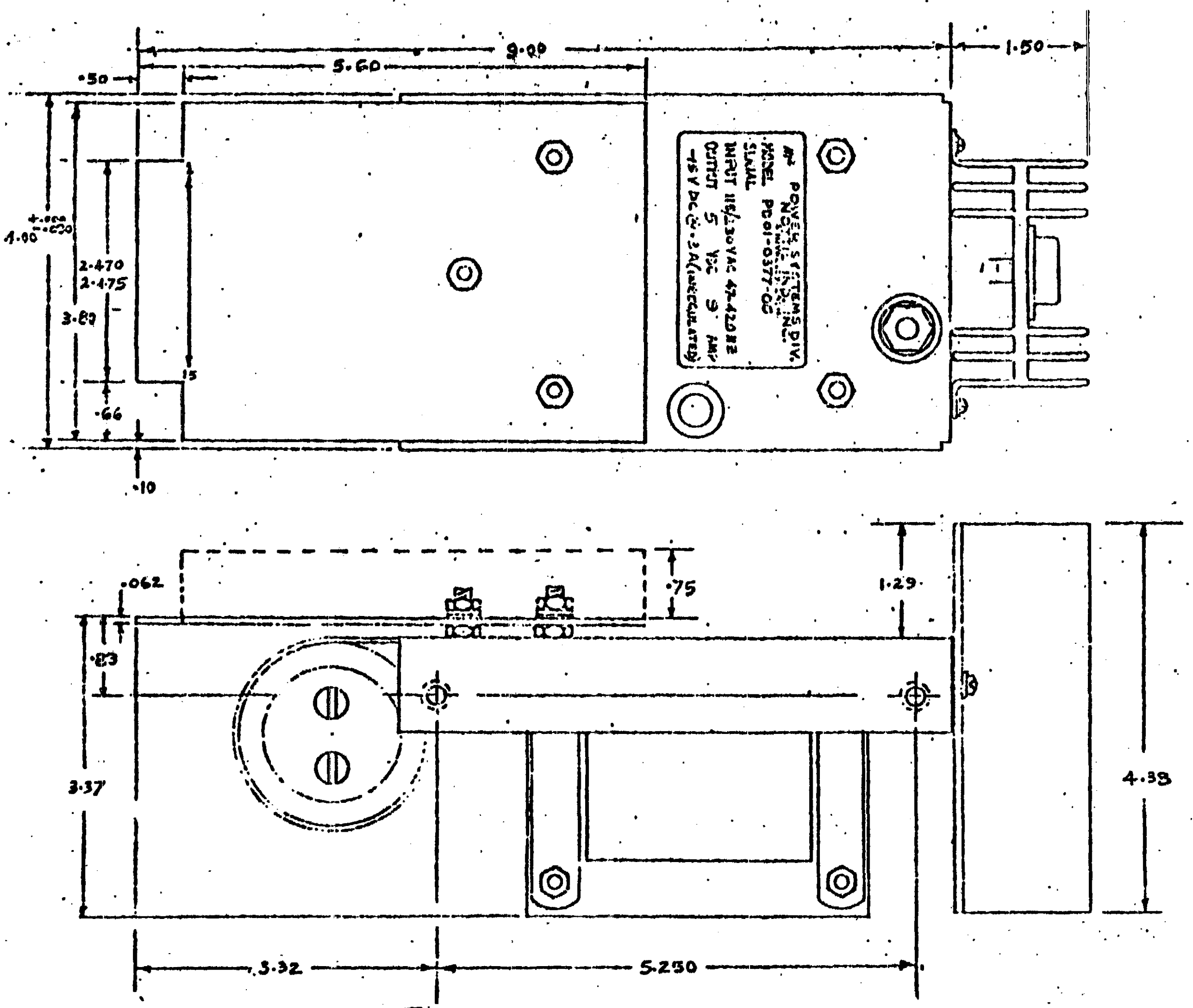
TITLE	WRITE CONTROL		
DWN	1/12/73	1/11	DES
CHK			ENGR
SCALE	—		FSC 31160
5-31-73			

Datum Inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

C 76193 E

SIZE SHT 2 OF 2 REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



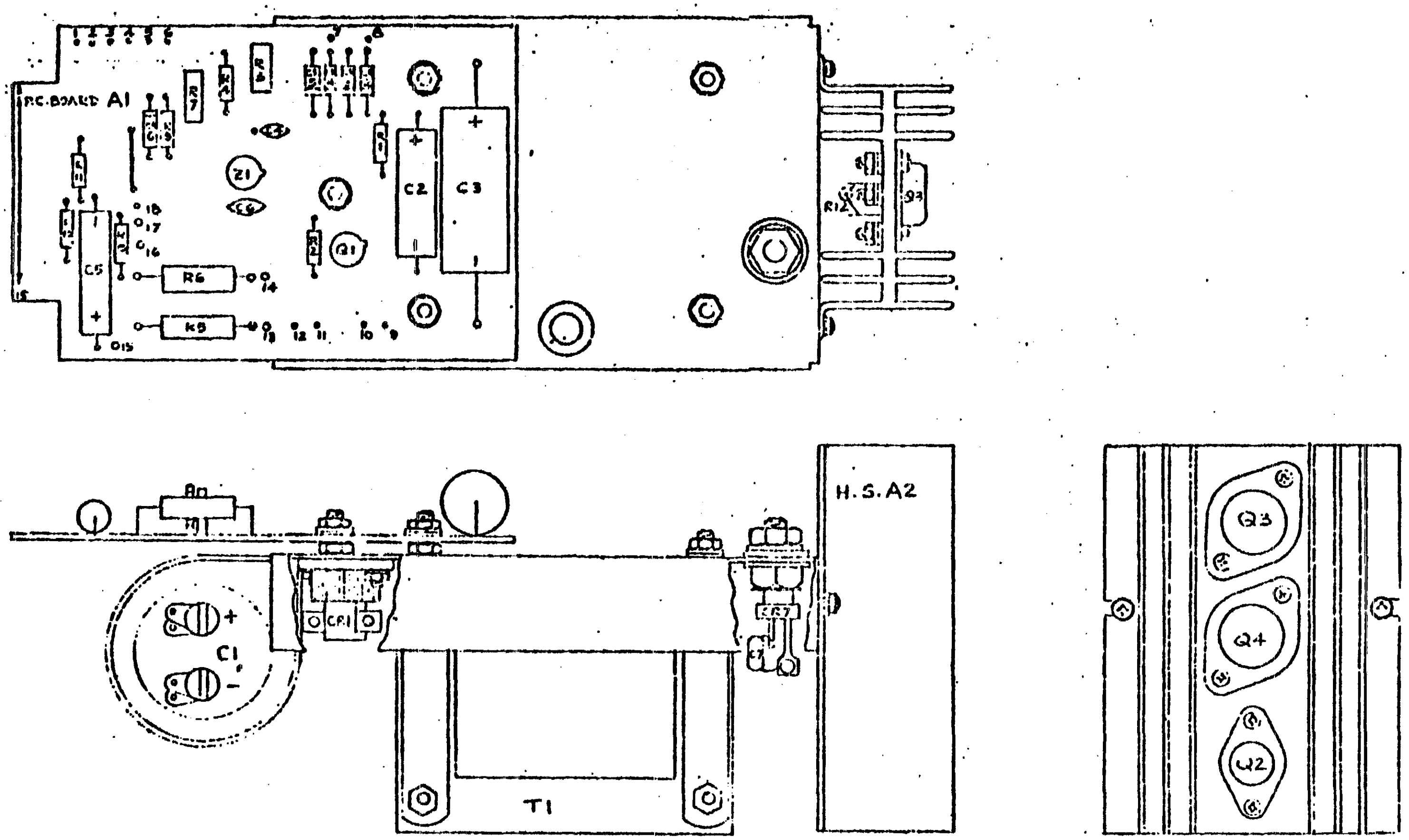
TITLE OUTLINE
POWER SUPPLY, +5VDC @ 9A
-15 VDC @ .2A

Datum Inc.
ANAHEIM, CALIFORNIA

94 0047

SH 1 OF 3

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



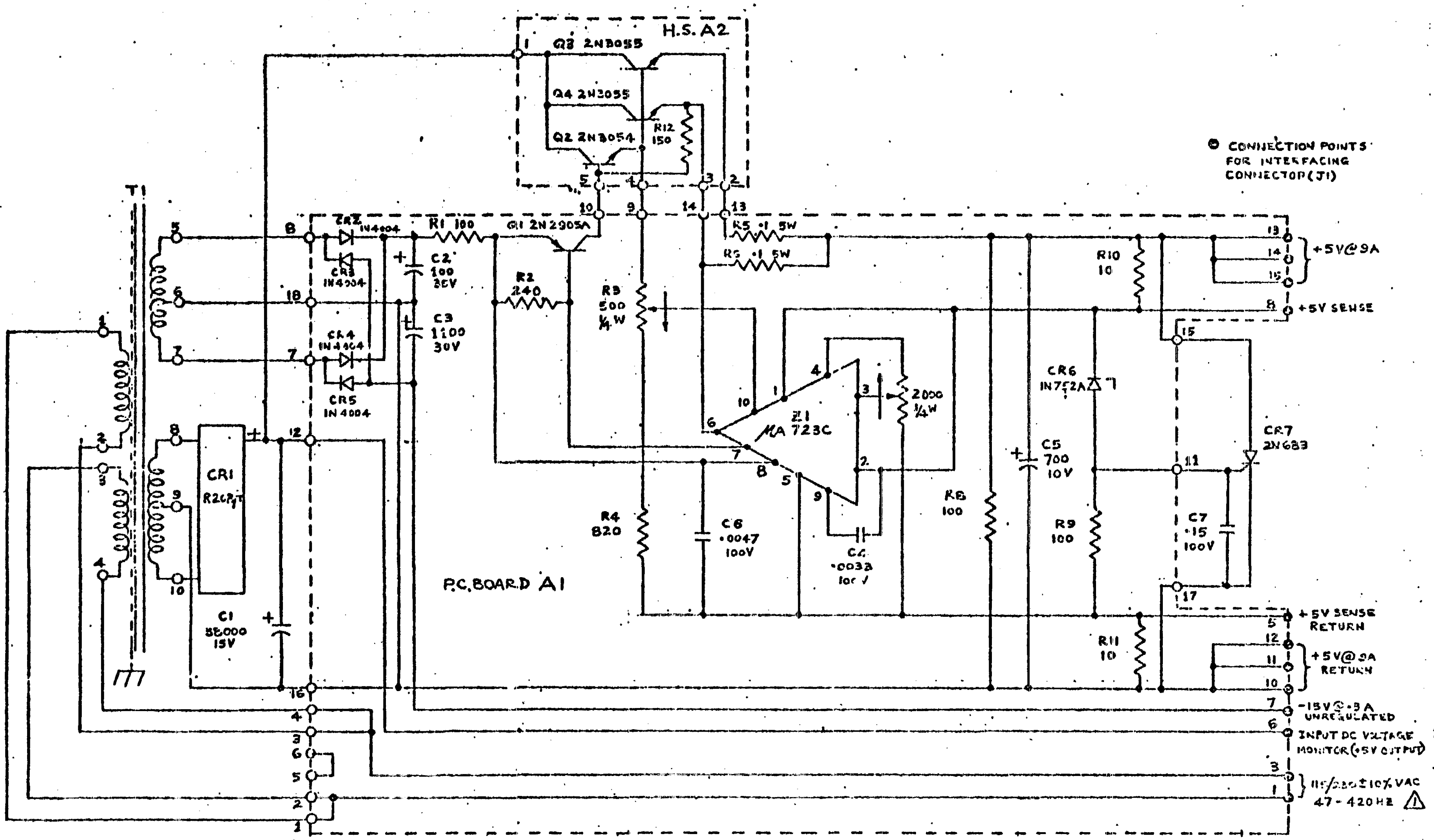
COMPONENTS LOCATION
POWER SUPPLY, +5V DC @ 9A
-15V DC @ 3A (UNREG.)

Datum Inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

943047

SCALE FULL | SHT 2 OF 3

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



3. ALL CAPACITORS ARE EXPRESSED IN MICROFARADS.
2. ALL RESISTORS ARE ½ WATT ±5%, EXPRESSED IN OHMS.
⚠ FOR 230 VAC OPERATION, REMOVE WIRES FROM A1-2, A1-3 ON P.C. BOARD AND PLACE ON A1-5 AND A1-6.
NOTES: UNLESS OTHERWISE SPECIFIED.

TITLE SCHEMATIC
POWER SUPPLY, +5V DC@9A, -15V DC @.3A

Datum Inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

940047

SH 3 OF 3

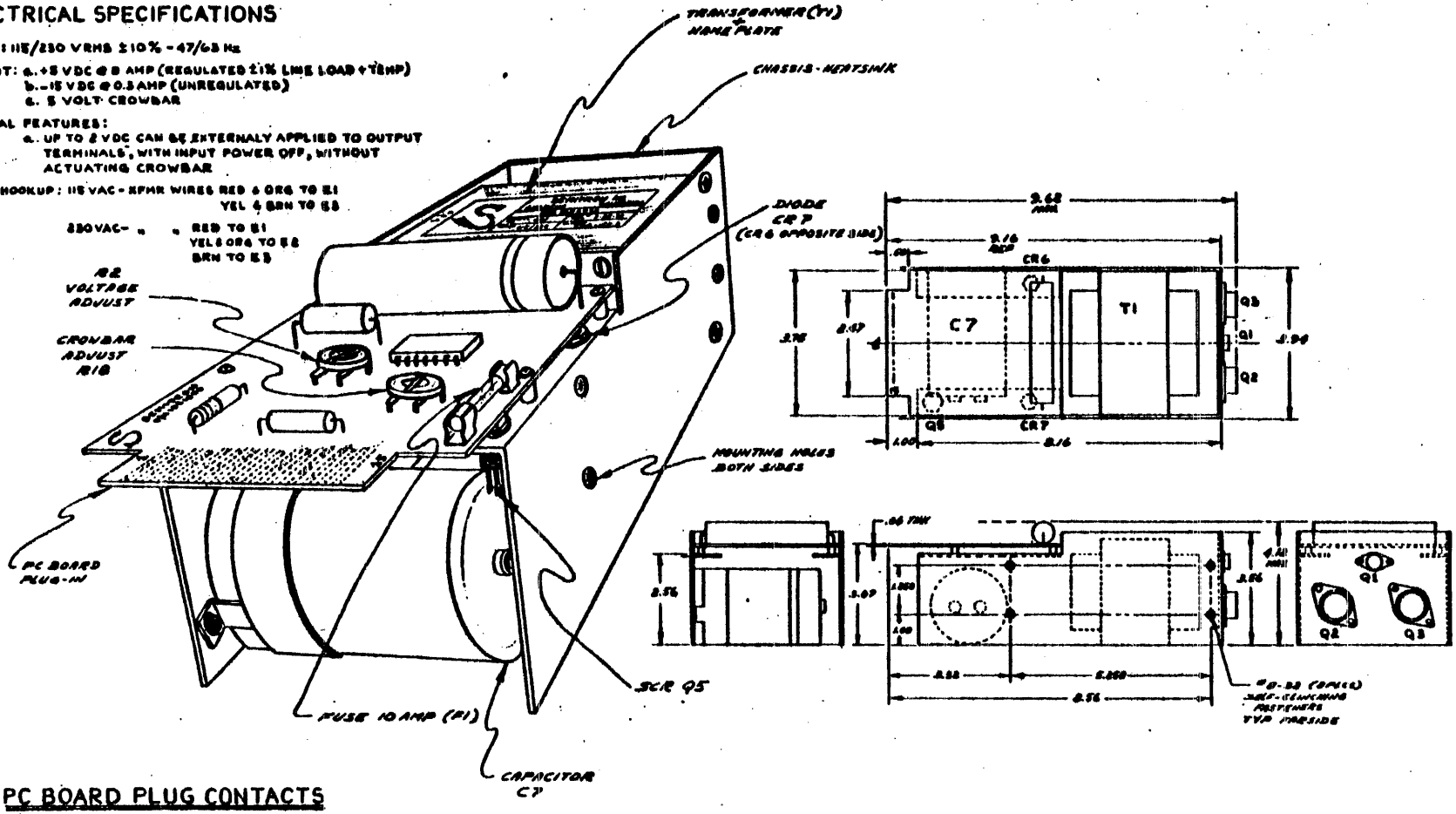
REVISIONS				
SYM	DESCRIPTION	BY	DATE	APPD
01	DRAWING RELEASE	TB	5/2/72	TB

I GENERAL SPECIFICATIONS

1. CASE FINISH-GOLD IRIDITE.
2. WEIGHT 8 POUNDS MAX.
3. TEMPERATURE 0°C TO 70°C CASE
4. PC BOARD PLUG CONTACTS - GOLD PLATED

II ELECTRICAL SPECIFICATIONS

1. INPUT : 115/230 VRMS ±10% - 47/63 Hz
2. OUTPUT: a. +5 VDC @ 8 AMP (REGULATED ±1% LINE LOAD + TEMP)
   b. -15 VDC @ 0.3 AMP (UNREGULATED)
   c. 5 VOLT CROWBAR
3. SPECIAL FEATURES:
   a. UP TO 8 VDC CAN BE EXTERNALY APPLIED TO OUTPUT TERMINALS, WITH INPUT POWER OFF, WITHOUT ACTUATING CROWBAR
4. INPUT HOOKUP: 115 VAC - XFMR WIRES RED & ORG TO E1
   YEL & BRN TO E3
   230 VAC - " " RED TO E1
   YEL & ORG TO E2
   BRN TO E3



PC BOARD PLUG CONTACTS

TIP 1 - 115/230 VAC
TIP 2 - NOT USED
TIP 3 - AC RETURN
TIP 4 - NOT USED
TIP 5 - 5V SENSE RETURN
TIP 6 - +5V UNREGULATED
TIP 8 - +5V SENSE
TIP 9 - NOT USED
TIP 10-12 - 5 V PWR RETURN
TIP 13-15 - +5V PWR 8 AMP

1. FOR SCHEMATIC REFER TO DWG NO. 1080500

NOTES: UNLESS OTHERWISE SPECIFIED

ITEM NO.	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	MATERIAL OR NOTE	QTY REQD
LIST OF MATERIALS OR PARTS LIST				

MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
FRACTIONS — DECIMALS — ANGLES
± 1/64 .xx = ± .02 ± 2°
.xxx = ± .010

DRN TB 5/2/72
CHK TB 5/2/72
APP 5/2/72
MODEL NO. 108
SCALE NONE

SEMITRON INC.
ANAHEIM, CALIF. 92806

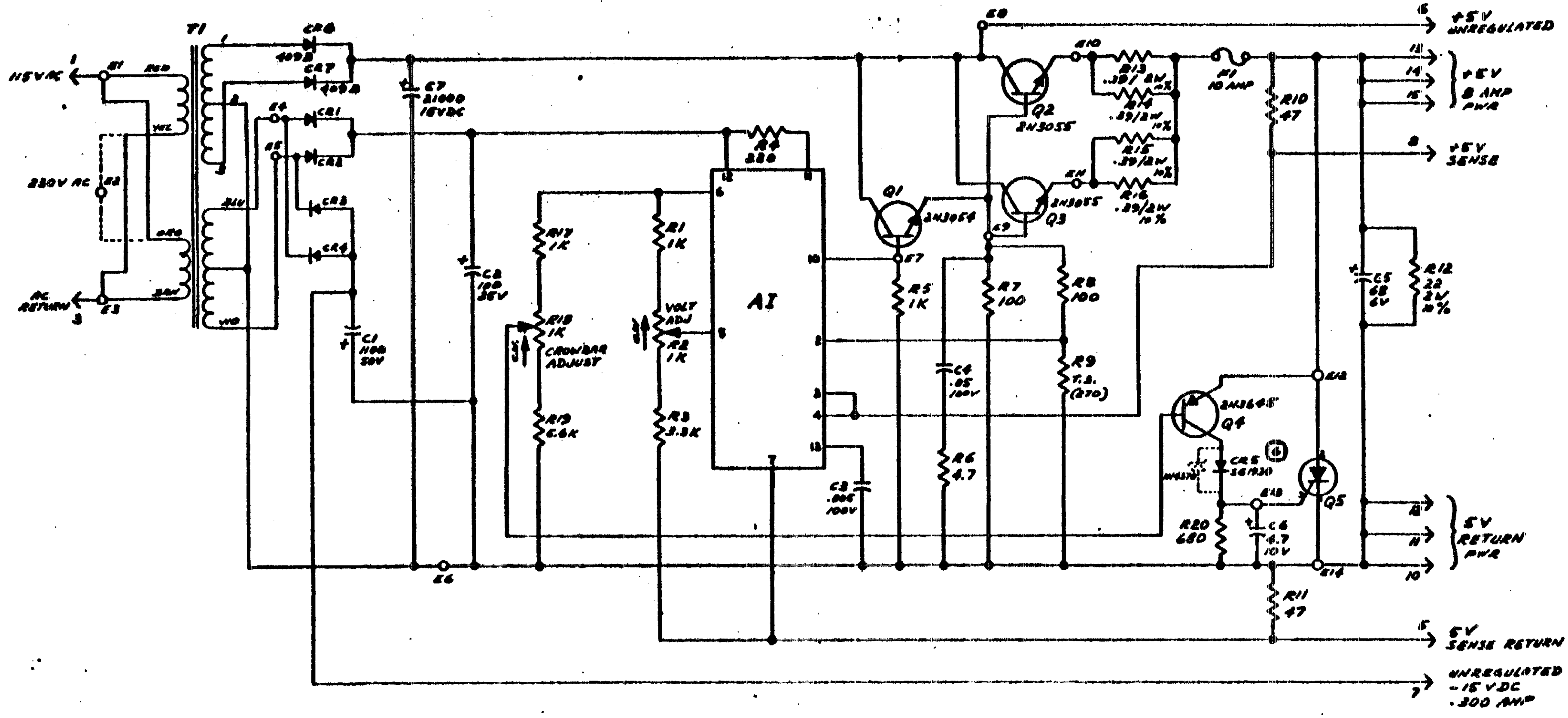
DRAWING TITLE
- OUTLINE DWG -
POWER SUPPLY
5 V DC @ 8 AMP (PLUG IN)

SIZE C | DRAWING NO. 1080000 | REV 01
SHEET 1 OF 1

QTY	USED ON	NEXT ASSY

REVISIONS

SYM	DESCRIPTION	BY	DATE	APPD
01	DRAWING & PRODUCTION RELEASE	T.B	1-25-72	T.B
02	CHANGED R20 TO CR5 & REDESIGNATED R21 TO R20 CR8 TO CR6 AND CR6 TO CR7; ADDED NOTE 6	T.B	2-8-72	T.B



Ⓖ REVERSE POLARITY WHEN REPLACING CR5 SG1930 WITH 1N4370 ZENER DIODE

5. ALL COMPONENTS ARE MOUNTED ON P.C.B. EXCEPT FOR T1, Q1 THRU Q3, Q5, C7 AND CR6 & 7
4. LAST REF. DESIGNATIONS T1, A1, Q5, C7, CR7, R20, F1 & E14
3. ALL DIODES ARE 1N4003
2. ALL CAPACITORS ARE RATED IN MICROFARADS
1. ALL RESISTORS ARE RATED IN OHMS, 1/2 WATT ± 5%

NOTES: UNLESS OTHERWISE SPECIFIED

ITEM NO.	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	MATERIAL OR NOTE	QTY REQD

LIST OF MATERIALS OR PARTS LIST

MATERIAL: SEE P/L 1085000	SEMITRON Inc. ANAHEIM, CALIF. 92806
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES FRACTIONS — DECIMALS — ANGLES ± 1/64 .XX = ± .03 ± 2° .XXX = ± .010	DRAWING TITLE: - SCHEMATIC - POWER SUPPLY 5 V DC @ 8A
DRN 12/8/71 · CHK 1/14/72 · APP 1/14/72	MODEL NO. 108 · SIZE C · DRAWING NO. 1080500 · REV 02
QTY — · USED ON 1085000 · NEXT ASSY —	SCALE NONE · SHEET 1 OF 1

WARRANTY

DATUM, Inc. guarantees this equipment to be free from defects in material and workmanship, for one year from date of delivery. Any repairs, or replacements (which alternative chosen by the manufacturer), will be carried out at the facilities of DATUM with transportation costs charged to the purchaser's account. Should a defect occur in equipment which cannot be returned feasibly because of physical size, or should the defect be trivial, the purchaser will be expected to perform first echelon repairs using materials supplied by DATUM. Subsequent repairs within the period of warranty will be negotiated separately.

If a defect should result from a design error, and both DATUM and the purchaser recognize this error as the cause of the defect, DATUM will correct the error to meet the specifications under which the equipment was delivered.

DATUM retains the right to return the defective equipment to the company's facilities for repair should this course be deemed necessary or advisable.

Equipment, accessories, batteries, and similar items not manufactured by DATUM are subject only to adjustments as can be obtained from the original supplier by DATUM. This warranty does not apply to any equipment, or portion thereof, which becomes defective through misuse, mishandling, or environmental conditions exceeding specifications, after delivery.

No other warranties, expressed or implied, shall apply to any equipment sold under this warranty, and the foregoing shall constitute the purchaser's sole rights under the agreed terms of this warranty.

In no circumstances shall DATUM assume liability for loss, damage or consequential expense arising directly or indirectly from the use of its equipment, separately, or in combination with other equipment.